Semiconductor Technologies for next Generation Mobile Communications

N. Collaert*, A. Alian, S.-H. Chen, V. Deshpande, M. Ingels, V. Putcha[1], A. Sibaja-Hernandez, B. van Liempd, A. Vais, A. Vandooren, A. Walke, L. Witters, H. Yu[1], D. Linten, B. Parvais[2], P. Wambacq[2] and N. Waldron

Imec, Kapeldreef 75, 3001 Heverlee, Belgium
[1]Also with KU Leuven, Leuven, Belgium
[2]Also with Vrije Universiteit Brussel, Brussels, Belgium
* Email: collaert@imec.be

Abstract

In this work, we will address the opportunities and technology challenges related to next generation mobile communication. To enable the required data rates and reliability for 5G applications, Si CMOS will need to be complemented with new materials and device architectures like III-V or GaN devices to enable at the same time the targeted speed and power efficiency of these systems. Heterogeneous integration, either monolithic or using 3D integration, will be a key enabler to achieve this.

1. 5G applications

5G is the next generation of mobile communication. Different from previous generations, the advent of 5G is expected to bring great new opportunities, and is seen rather as a revolution than an evolutionary improvement over 4G-LTE.

The expectation for 5G is that it will enable extreme mobile broadband with peak data rates up to 10Gbps and even higher, massive machine-to-machine communication to support the Internet-of-Things (IoT) platform and critical machine communication (e.g. autonomous driving) with ultra-high reliability and latencies below 1ms [1]. To enable this, not only innovations in the network infrastructure, with the introduction of small cells (e.g. femto, pico cells,...), will be needed but also in the technologies for the mobile devices themselves, with in first instance smartphones as dominant devices responsible for more than 80% of all mobile traffic.

While first 5G roll-out is expected by 2020 [2], 5G is expected to be introduced in several phases with long deployment cycles. Addressing first the sub-6GHz frequency bands, which include the traditional cellular bands, next phases will target the mm-wave bands, starting with 28GHz [3]. The large amount of available spectrum is the primary reason for the high interest in the mm-wave spectrum. Larger channel widths up to 500MHz and even 1GHz are also expected for these high frequency bands. Both sub-6GHz and mm-wave frequency bands will need to be enabled in one common architecture and devices will probably need to access both bands simultaneously. This translates into the use of higher speed devices than what is currently considered for 4G-LTE. Next to that, the form factor and battery lifetime restriction in small cells and mobile devices require the power consumption of these mm-wave circuits to be kept limited. Especially the transmit circuitry, that typically consumes most of the power in a radio, needs to operate at a high efficiency with devices that have better power handling capabilities over standard CMOS.

Finally, the increased amount of carrier frequencies, the further deployment of carrier aggregation and MIMO, massive Multiple-Input-Multiple-Output communication, will require the enablement of complex RF front-end modules (RF-FEM) with a higher degree of integration. Figure 1 shows a schematic representation of the diverse technology needs for the RF-FEM, RF transceiver and digital modem. In today's RF systems, several integrated circuits (IC), that are based on widely different semiconductor processes, are used to address the different functionalities of each of the blocks. Moving to 5G, an increasing number of switches, filters, power amplifiers (PA) etc. will be needed for the RF-FEM and this will pose a significant challenge to design circuits that can fulfill the form

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factor and power efficiency requirements of mobile handheld devices. Heterogeneous integration where these dissimilar technologies are more closely integrated and connected will be a key enabler to bring mm-wave functionality in handheld devices.

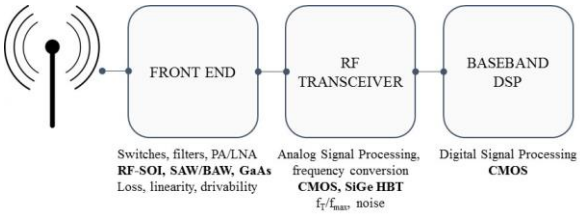

Figure 1. Schematic representation of an RF system indicating the different blocks, technologies and figures-of-merit (FOMs)

In the next sections we review the most promising device architectures and possible heterogeneous integration schemes to address the requirements for next generation RF technologies.

2. Challenges for Si CMOS

Nowadays Si CMOS technology is moving to the 3nm technology node. With many challenges to maintain power and performance gains of the digital circuits at these small dimensions, process innovations like the use of efficient stressors, low-k spacers, low contact resistivity materials and methods, new channel materials like (Si)Ge and innovations in BEOL are mandatory to keep on the trendline, set by Moore's law. Advanced devices like FinFET and Gate-All-Around (GAA) transistors are primarily developed for logic applications, however, they are also used in the analog/RF parts of Systems On Chip (SOCs) where different requirements are desired for the analog/RF circuits.

When evaluating and comparing the speed of different device architectures, one typically looks at FOMs like f_T and f_{max}, which represent the unity current gain frequency and maximum oscillation frequency, respectively:

$$f_t \approx \frac{g_m}{2\pi\left[\left(C_{gs}+C_{gd}\right)\left(1+g_d\left(R_s+R_d\right)\right)+C_{gd}g_m\left(R_s+R_d\right)\right]} \approx \frac{g_m}{2\pi C_{gg}} \quad (1)$$

$$f_{max} \approx \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)\sqrt{4g_d\left(R_g+R_s+R_i\right)+2\frac{C_{gd}}{C_{gs}}\left(g_m\left(R_s+R_i\right)+\frac{C_{gd}}{C_{gs}}\right)}} \approx \frac{f_t}{2\sqrt{g_d\left(R_g+R_s+R_i\right)+2\pi f_t R_g C_{gd}}} \quad (2)$$

with C_{gs}, C_{gd}, C_{gg} the gate-source, gate-drain and gate capacitance; g_d the drain conductance; g_m the transconductance; R_g, R_s, R_d the gate, source, drain resistance.

Figure 2 compares the f_T and f_{max} performance of different Si CMOS technologies. Whereas most advanced high-k/metal gate planar bulk and FDSOI technologies show numbers well above 300GHz, most advanced FinFET technologies are lagging behind in performance.

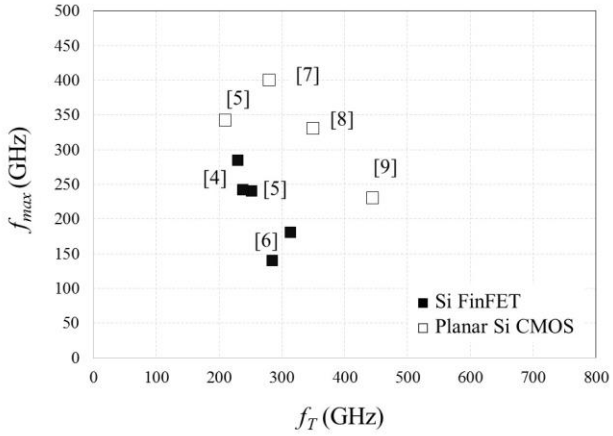

Figure 2. f_{max} versus f_T comparison of different Si CMOS technologies.

The increased parasitics in FinFET, especially the higher R_g has a detrimental impact on the device speed (see e.g. eq. 2 of f_{max}). This issue has been addressed in a number of reports, showing that further improvement of the FOMs is possible [5, 6]. The use of a double-sided gate contact and the reduction of the number of fins are both beneficial to reduce the gate resistance and increase f_{max}.

However, increasing the speed of FinFET devices remains all in all challenging, especially when considering further downscaling where increased parasitic capacitance due to spacer scaling, increased access resistance due to contact area scaling and gate resistance increase due to the limited space for gate fill metals and the 3D-nature of the device will dominate the overall performance of the transistor [10].

3. III-V and GaN devices

III-V materials have been a topic of interest during the last decade, mostly as an alternative to replace the Si channel in scaled technology nodes for logic applications [11, 12]. Although reports have shown that challenges related to gate stack reliability [13], defectivity and scalability make them less suitable for ultra-scaled logic transistors, their intrinsic higher mobility and injection velocity together with a High Electron Mobility Transistor (HEMT), MOS-HEMT (using a buried channel with MOS gate stack) or even Heterojunction Bipolar Transistor (HBT) architecture make them ideal candidates for RF applications. This is illustrated by comparing the f_{max} values of different III-V devices with silicon ones (see Figure 3). Devices with the highest f_T/f_{max} have been shown for (In)GaAs-based HEMTs and HBTs.

More so than speed, the available output power (P_{out}) and power added efficiency (*PAE*) of RF-FEM power amplifiers will be key for 5G handheld devices. In [14], the power handling capabilities of GaN, GaAs, SiGe and CMOS are compared, showing that both at low frequencies (sub-6GHz) and mm-wave GaN and GaAs devices outperform SiGe and CMOS. This can be exploited for example in beamforming radio architectures that are going to be used in the mm-wave part of 5G: here different antennas in an array are each driven by a power amplifier. A higher P_{out} and *PAE* mean lower amount of elements needed to drive the antennas and more energy-efficient systems can be enabled.

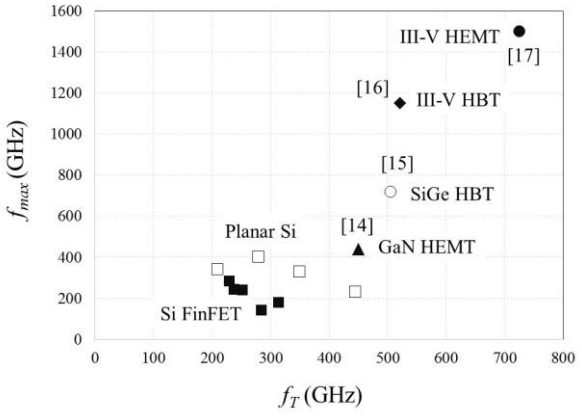

Figure 3. f_{max} versus f_T comparing Si CMOS technologies to SiGe HBT, GaN and (In)GaAs devices.

While originally considered for high-voltage applications [18], GaN with its unique properties combining a high sheet charge due to the efficient polarization effect and its wide bandgap, is now also finding its way to the RF market, even for applications beyond base stations like handsets where much reduced voltages are required.

Recent work shows significant progress in improving the speed of these devices [14], suggesting that highly scaled GaN transistors are excellent candidates for next generation 28 GHz and higher 5G mobile bands where Si CMOS has difficulties achieving the required output power. Challenges for GaN are related to upscaling these devices to 200mm and even 300mm Si platforms, scalability and performance at reduced bias voltages.

4. Heterogeneous integration

Finally, co-integration either on the same substrate [19] or through 3D stacking will be required to enable these heterogeneous systems combining advanced CMOS and dedicated RF devices. Next to Through-Silicon-Via (TSV) based or wafer-to-wafer bonding 3D technologies, sequential 3D has gained a lot of attention in last years. The potential to integrate smaller sized interconnects with high density and shorter length between the different tiers, and the reduced area have been the main drivers to look into this technology. In [20], planar Si junction-less RF devices have been demonstrated on bulk Si using this technology (Figure 4). No impact of the device stacking has been seen and the RF performance of the devices is in line with the expected $1/L_G$ dependence of f_T. This first demonstration shows the way to build dedicated top tier devices with different materials and architectures and combine them with advanced CMOS devices that provide the logic functionality.

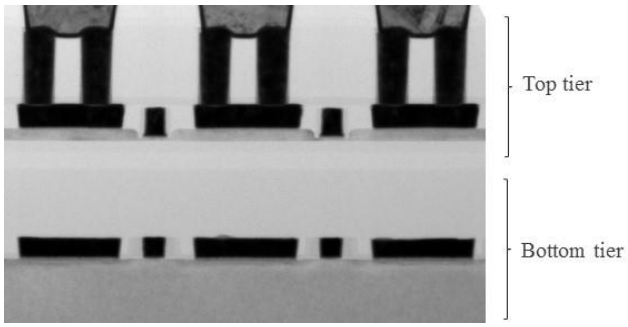

Figure 4. TEM picture showing stacked Si RF devices.

5. Conclusions

(In)GaAs and GaN devices are promising technologies to enable next-generation mobile communication systems. Especially for RF-FEMs in handheld devices which are both restricted in form factor and battery lifetime, these technologies can bring both the required speed and power handing capabilities. Ultimately these devices will need to be co-integrated with advanced CMOS. Co-integration, either on the same substrate (monolithic integration) or through 3D stacking, will be key enablers for these heterogeneous systems. This will also bring the interaction between design and technology to a next level: system-technology co-optimization (STCO) where optimization is done across many different levels, from process unit steps and integration up to the application level.

Acknowledgments

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