

# Recent Progress in GaN Device Technology

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## Abstract

Several new technologies for GaN high frequency devices and GaN power devices are reviewed. Newly developed GaN devices have a superior performance over conventional Si-based ones in view of lowering the energy loss and reducing the system size. Normally-off GaN HFETs are demonstrated.

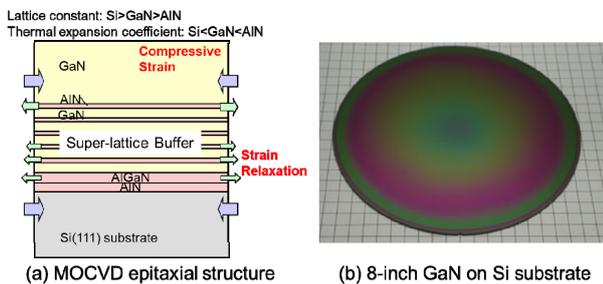
## 1. Introduction

GaN-based devices are considered a viable alternative for conventional Si-based ones due to superior blocking voltage and higher current characteristics. The trend of saving energy has gradually shifted the GaN-based devices toward the development of efficient power electric systems. At present, a variety of power applications have been realized by using GaN hetero-junction field effect transistors (HFETs) having low on-resistance and superior switching capabilities. Highly efficient power converter system will be one of the promising applications of GaN HFETs.

## 2. Features of GaN HFETs

### 2.1 GaN on silicon epitaxial growth technology

GaN epitaxial growth on silicon substrate is a viable technology in the cost point of view [1]. The advantage of Si substrate is that 8-inch large diameter substrate is available, by which we can use the payout Si facilities. GaN on Si epitaxial structure is shown in Fig. 1(a). AlGaIn/AlN initial layer and GaN/AlN super-lattice structure are introduced. Photograph of an 8-inch GaN on Si substrate is shown in Fig. 1(b). Crack-free and mirror surface was achieved. High mobility characteristics with good uniformity were also realized.

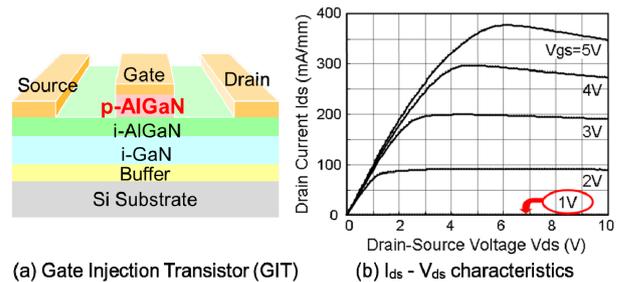


Figures 1. (a) GaN on Si epitaxial structure, (b) Photograph of an 8-inch GaN on Si substrate.

### 2.2 Normally-off operation of GaN HFETs

p-AlGaIn/AlGaIn/GaN HFETs named the gate injection transistor (GIT) enables normally-off operation of GaN on Si HFETs [2]. The p-type AlGaIn gate is used instead of conventional Schottky one, as shown in Fig. 2(a). Naturally formed two-dimensional electron gas (2DEG) which is generated by the material polarization at the interface of i-AlGaIn and i-GaN is depleted owing to the potential lift by p-type gate barrier. The current ( $I_{ds}$ ) - voltage ( $V_{ds}$ ) characteristics of GaN GIT are the same as the enhancement-mode FETs, as shown in Fig. 2(b).

High efficient inverter system for motor drive is promising application of GaN GIT. Low loss operation was realized in GaN GIT inverter system. A 99.3% of power conversion efficiency in GaN GIT inverter system was achieved at 1500 W, as shown in Fig. 3.



Figures 2. (a) Schematic cross-section of GaN GIT, (b)  $I_{ds}$ - $V_{ds}$  characteristics of GaN GIT.

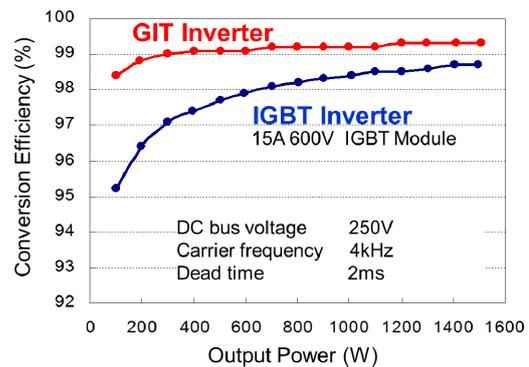


Figure 3. Power conversion efficiency in GaN GIT inverter system and that in IGBT inverter system.

### 3. Recent progress in GaN Device Technologies

#### 3.1 Bi-directional GaN GIT for 3×3 matrix converter

The GaN GIT structure shown in Fig. 2(a) can be easily turned into a monolithic bi-directional GaN GIT by providing the double gates between source and drain regions, as shown in Fig. 4. The bi-directional GaN GIT directly switches AC power with small series resistance [3]. The bi-directional GaN GIT expands the power electronics application, such as inverters with no free-wheel diode, DC/DC converters, and monolithic AC-AC matrix converters. With using bi-directional GaN GIT, low on-resistance and high break down voltage characteristics were achieved, as shown in Figs. 5. Free from the on-state voltage offsets at on-state enables low loss operation, as shown in Fig. 5(a). The on-state resistance ( $R_{on}$ ) was 42 mΩ with the maximum current ( $I_{S2}$ ) of 100 A.

Matrix converter which directly transduces power and frequency is expected to be a winning AC to AC converter due to capacitor-free circuit configuration. System block of GaN 3×3 matrix converter using bi-directional GaN GIT is shown in Fig 6.

Output line voltage and output phase current of the GaN 3×3 matrix converter are shown in Fig. 7. Smooth output phase current was obtained.

The operation loss of GaN 3×3 matrix converter decreased a half from 120 W to 60 W at total output power of 1.8 kW, compared with that of IGBT one [4]. The maximum efficiency increased from 94% to 98% at output power of 1.0 kW.

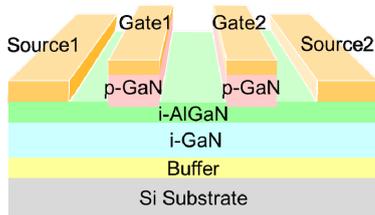
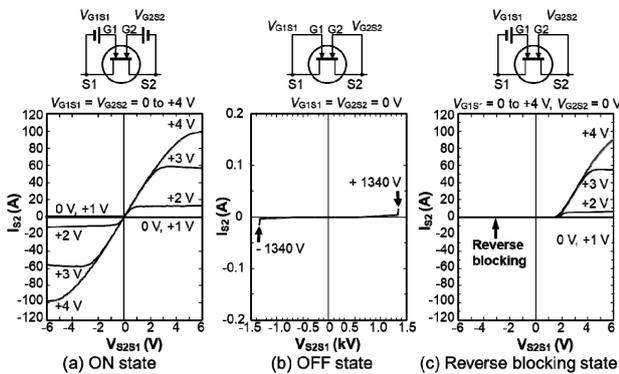


Figure 4. Schematic cross-section of monolithic bi-directional GaN GIT.



Figures 5.  $I_{S2}$ - $V_{S1S2}$  characteristics of bi-directional GaN GIT.

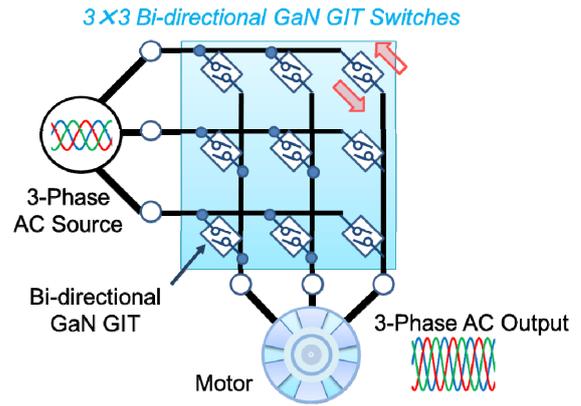


Figure 6. System block of GaN 3×3 matrix converter.

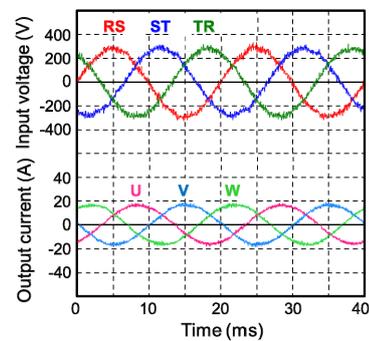


Figure 7. Output line voltage and output phase current of GaN 3×3 matrix converter.

#### 3.2 Normally-off NiO gate AlGaIn/GaN MOS-HFET

In order to realize normally-off GaN metal-oxide-semiconductor (MOS) HFETs, NiO gate AlGaIn/GaN MOS-HFETs on Si substrate were proposed [5]. The structure of NiO/AlGaIn/GaN MOS-HFETs is shown in Fig. 8. Selectively deposited NiO gate layer using atomic layer deposition (ALD) technique contributed to shorten the spacing between source and drain regions. NiO/AlGaIn/GaN MOS-HFETs realized normally-off characteristics even with the 30% Al mole fraction of i-AlGaIn layer [6].

In order to realize extremely low  $R_{on}$ , a Ge-doped  $n^{++}$ GaN layer was introduced for ohmic contact to reduce contact resistance. Highly n-type doping technique was developed using Ge as a dopant in regrowth by metal organic chemical vapor deposition (MOCVD). Carrier concentration over  $1 \times 10^{20} \text{ cm}^{-3}$  was achieved, while Si doping has a limitation in a doping concentration range as high as  $2 \times 10^{19} \text{ cm}^{-3}$ . Extremely low specific contact resistance of  $1.5 \times 10^{-6} \Omega \cdot \text{cm}^2$  was achieved.

Figure 9 summarizes the processing steps of device fabrication of the NiO/AlGaIn/GaN MOS-HFET. The cross sectional scanning electron microscope (SEM) image of the NiO/AlGaIn/GaN MOS-HFET is shown in Fig. 10.

The current-voltage characteristics are shown in Figs. 11. Figure 11(a) shows extremely low  $R_{on}$  of  $0.95 \Omega \cdot \text{mm}$ . A positive threshold voltage ( $V_{th}$ ) of  $0.55 \text{ V}$  realized normally-off operation, as shown in Fig. 11(b). Maximum drain current ( $I_{ds}$ ) of  $1.1 \text{ A/mm}$ , off-state current of  $2 \times 10^{-7} \text{ A/mm}$ , trans-conductance ( $g_m$ ) of  $490 \text{ mS/mm}$  were achieved.

Figure 12 shows NiO/AlGaIn/GaN MOS-HFET characteristics comparing those reported  $R_{on}$  of normally-off GaN HFETs as a function of drain source distance ( $L_{sd}$ ) [7-9]. As was extracted by the typical modeling technique, contact resistances ( $R_c$ ) at source and drain electrodes reached down to as low as  $2 \times R_c$  of  $0.23 \Omega \cdot \text{mm}$ .

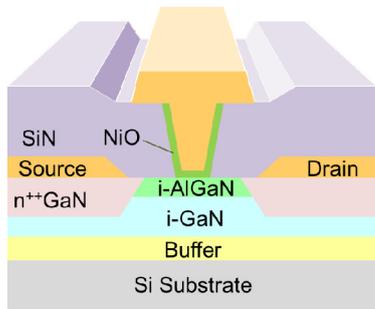
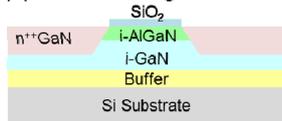
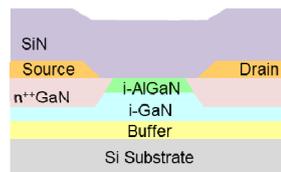


Figure 8. Schematic cross-section of NiO/AlGaIn/GaN MOS-HFET.

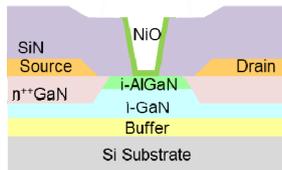
(a) Selective regrowth of  $n^{++}\text{GaIn}$



(b) SiN deposition



(c) NiO selective deposition



(d) Gate metal deposition

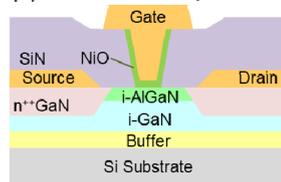


Figure 9. Fabrication process of NiO/AlGaIn/GaN MOS-HFET.

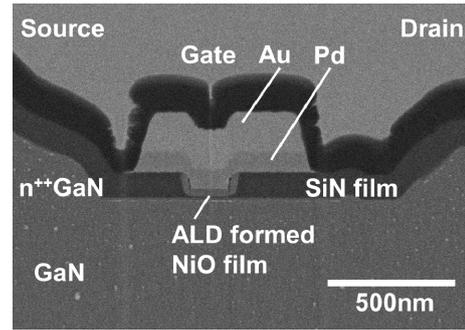


Figure 10. Cross sectional SEM image of NiO/AlGaIn/GaN MOS-HFET.

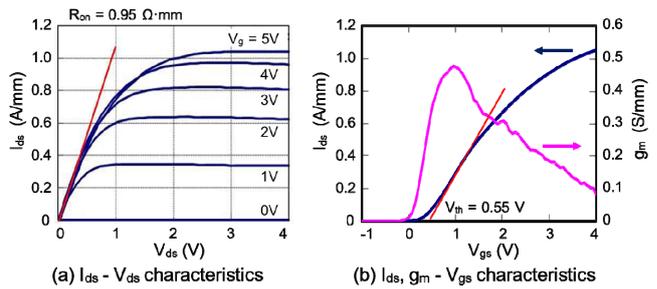


Figure 11. (a)  $I_{ds}-V_{ds}$ , (b)  $I_{ds}, g_m-V_{gs}$  characteristics of NiO/AlGaIn/GaN MOS-HFET.

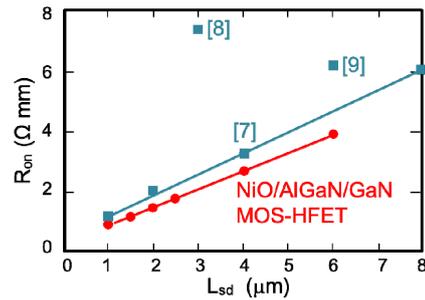


Figure 12. Reported  $R_{on}$  of normally-off GaN HFETs.

### 3.3 Normally-off AlON gate AlGaIn/GaN MIS-HFET

High current and high voltage AlGaIn/GaN metal-insulator-semiconductor (MIS) HFETs using AlON gate insulators were demonstrated [10]. Figure 13 shows the structure of the AlON/AlGaIn/GaN MIS-HFETs on Si substrate.

A schematic summary of the processing steps of device fabrication of the AlON/AlGaIn/GaN MIS-HFET is shown in Figs. 14. An AlGaIn thin layer is epitaxially grown over the grooved structure of the AlGaIn/GaN, as shown in Fig. 14(b). AlON is formed over the regrown surface by ALD that offers the better uniformity and less processing damage [11]. An oxygen annealing followed by the deposition of AlON results in the positive shift of  $V_{th}$ , enabling the normally-off operation.

The maximum drain current reached 20 A at the gate voltage of 10 V. The gate width of the device was 100  $\mu\text{m}$ . The  $R_{\text{on}}$  was as low as 270 m $\Omega$  that was 84 % reduced by introducing the recessed gate structure.

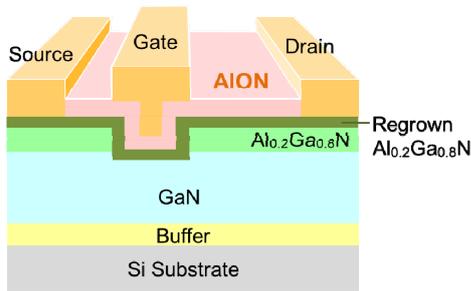
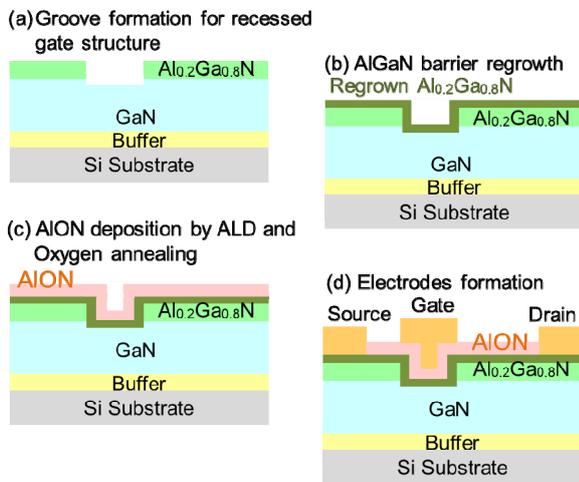


Figure 13. Schematic cross-section of AION/AlGaIn/GaN MIS-HFET.



Figures 14. Fabrication process of AION/AlGaIn/GaN MIS-HFET.

### 3.4 Fusion of Power and RF device technologies

The historical map of Panasonic GaN-based devices in both Power and RF application fields is shown in Fig. 15. The fusion of power device technology and RF device technology was realized in the GaN devices.

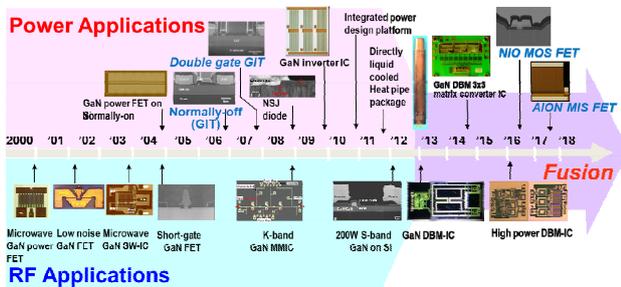


Figure 15. GaN device development history in Power and RF application fields.

## 4. Summary

Several new technologies for GaN devices were reviewed. Developed GaN devices have superior performance to the conventional Si ones in view of lowering the energy loss as well as reducing the system size. We believe the fusion of power device technology and RF device technology will open "Green" power electronics in the future.

## Acknowledgments

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