Design, Fabrication and Characterization of Ultra-High Voltage 4H-SiC MOSFET Transistors

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Abstract
A 10-kV silicon carbide MOSFET transistor with multi-zone gradient guard ring (MZG-GR) structure is designed, fabricated, and analyzed. Design and optimization based on two-dimensional device simulator TCAD is used to investigate the effects of MZG-GR technique on breakdown for SiC MOSFET devices. It is found that MZG-GR can achieve a maximum blocking voltage owing to alleviated electric field crowding in the periphery of the active area. Moreover, optimized MZG-GR structure exhibits good tolerances to total dose and surface charges. For the SiC MOSFET transistors with a 100 μm thick epi-layer doped to 5×10^{14} cm^{-3}, a measured breakdown voltage achieved is 13.6 kV at a source-drain current of 0.01 mA, corresponding to about 95% of the ideal value for a 1-D structure. Furthermore, the variation in reverse blocking voltage with respect to the ring spacing observed in the fabricated transistors shows a good agreement with the simulated results in the trend.

1. Introduction

Ultra-high voltages (>10 kV) MOSFETs (metal oxide semiconductor field effect transistors) based on silicon carbide (SiC) are the future alternative to silicon for high-power, high-temperature, high-frequency electron devices thanks to the superior physical properties like high breakdown electric field and large thermal conductivity [1]. Up to now, 10 kV 4H-SiC power MOSFETs is becoming available, which will reduce the complexity of megawatt power systems because of the simpler topologies with fewer levels and realization of new applications, such as grid systems, railway traction converters, and high-power renewable energy conversion and storage [2-3].

For ultra-high voltage devices, periphery protection is mandatory in order to reduce the well-known electric field crowding taking place at the junction edge. Nowadays, many planar junction termination technique have been employed to obtain an ultimate performance of SiC materials [4-6]. Junction termination extensions (JTE), guard rings (GR) and field plate (FP) have been successful for SiC power device to solve the periphery problems. However, the impurity dose of JTE region is sensitively depend on the activation condition of ion implantation. This method is hard to optimize and usually require multi-zone JTE structure to obtain the maximum breakdown voltage. GR is often difficulty to optimize and fabricated owing to the strongly coupled function between the breakdown voltage and each ring. In recent years, several methods to realize multiple-zone JTE have been reported. However, fabrication of multi-zone JTE structure in SiC requires multiple masked ion-implantations or one more etching step, which will increase the processing complexity.

Design, fabrication and analysis of multi-zone gradient guard ring technique for 10kV 4H-SiC MOSFETs are presented in this work. The MZG-GR is employed to obtain a maximum breakdown voltage by lowering the amount of electric field crowding at periphery of proposed structure, thus improving reliability. Compared with SiC device with the equally spaced guard ring, the proposed structure with breakdown voltage of 13.6 kV exhibits a more than 40% improvement in the reverse blocking characteristics. Meanwhile, the simulated and experimental results of the number and spacing of rings dependence of the breakdown voltage are also compared and discussed.

2. Physical Model, Device Structure and Fabrication

2.1 Physical Model

In this paper, the 2-D analyzed works for 10kV devices has been conducted using Silvaco TCAD, including models for energy bandgap narrowing, recombination, impact ionization, mobility, incomplete ionization of impurities, and lifetime. The primary parameter of the 4H-SiC material for both electrons and holes in the simulation software are summarized in Table 1, which is taken from the recent literature.

Table 1. Simulation model parameters assumed at room temperature

Material parameter	Unit	Value
band gap energy, E_g (300K)	eV	3.26
$\tau_{n,p}$	s	1×10^{-6}, 2×10^{-7}
acceptor energy level, E_{AB}	meV	191
donor energy level, E_{DB}	meV	65

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minimum mobility values (electron and hole), $\mu_{0n,p}^{min}$	$cm^2/V{\cdot}s$	40, 15.9
maximum mobility values (electron and hole), $\mu_{0n,p}^{max}$	$cm^2/V{\cdot}s$	900, 124
degeneracy factors for conduction and valence bands, G_{CB}/G_{VB}		2/ 4
saturation velocity, v_{sat}	cm/s	2×10^7

2.2 Device Structure and Fabrication

A simplified cross-section view of the fabricated 10kV-class 4H-SiC MOSFET transistor with MZG-GR structure is illustrated in Figure 1.

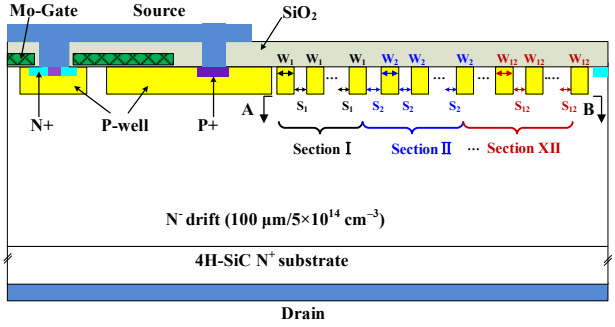

Figure 1. Schematic cross-sectional view of proposed MOSFET transistor using MZG-GR technique.

In this work, a 100-μm thick N-type epi-layer with the concentration of 5×10^{14} cm^{-3} on a Si-faced N^+ type 4H-SiC wafer is selected to sustain the 10kV breakdown voltage. The channel length is fixed to 2μm, and the JFET width is set to 4μm. The main junction and guard rings at the periphery are formed simultaneously. Multiple Al and N ion implantation at 500°C are used to form P-type and N-type region, and the implant blocking layer is a carbon cap. High temperature anneal (1800°C and 10 min) for all implant species is required to reach a significant amount of electrical activation. Thermal oxidation and gate-oxide nitridation in N_2O ambient at 1300°C for 7 hour is applied to improve the quality of the SiC/SiO_2 interface, , following Mo layer and Ti/Ni film are deposited for the gate , source and drain contact respectively. Subsequently, rapid thermal annealing is done at 1000°C for 2 min in N_2 ambient to form the ohmic contacts on the source and drain terminal. In order to reduce the surface leakage current and to avoid sparking in air, the silicon dioxide layer and a thick polyimide layer are deposited as first and secondary passivation layer. The edge termination of SiC MOSFET with MZG-GR structure is divided into 12 zones, and each zone includes 11 equally spaced rings of 3 μm width. And the spacing between P implantation rings ($S_{1..12}$) in the zone linearly increased from 1.3 μm to 3.5 μm. To experimentally verified and comparison, the SiC MOSFET transistor with equally spaced GR (S_{con} = 2 μm) as well as various active area are also fabricated on the same wafer. The optical microscopic image of fabricated SiC MOSFET with MZG-GR structure is shown in Figure 2.

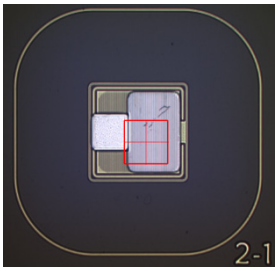

Figure 2. Optical microscopic image of 4H-SiC MOSFET transistor with MZG-GR structure.

3. Discussion

3.1 Off-State characteristics

Figure 3 illustrates the wafer-level off-state characteristics at 300 K for proposed 4H-SiC MOSFET transistors with 12-zone and S_1=1.3μm. The test chips are immersed in Fluorinert oil due to electrical arching in air. As can be seen from this figure, the MZG-GR structure with the measured reverse blocking voltage of 13.6 kV could achieve to 95% of the ideal PN junction breakdown voltage [7-8].

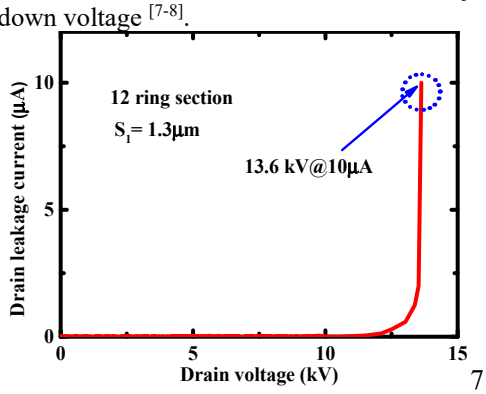

Figure 3. The measured blocking voltage of MZG-GR device with 12-section and S_1=1.3μm.

Figure 4 shows the comparison of the off-state characteristics of SiC MOSFETs with MZG-GR and the equally spaced GR structures. It is found that the typical breakdown voltage is only 9.7 kV for SiC MOSFET with uniform spacing structure (S = 2 μm), but is increased by 40% and 25% to 12.1 kV (S_1=1.5 μm) and 13.6 kV (S_1=1.3 μm) by applying multi-zone gradient guard ring technique. This is because that the lateral reduction of effective charges in MZG-GR structure decreases electric field strengthen in the p-n junction, thus making the junction less vulnerable to high voltage breakdown and current leakage when reverse biased.

Figure 5 presents a comparison of the simulated surface electric field distribution along A-B cutline in Figure 1 for different applied reverse voltages. For the equally spaced GR structure, the electric field shielding of the main junction is diminished and breakdown voltage is

lowered. It is obvious from this graph that the peak electric field of 3 MV/cm occurs at the innermost ring for equally spaced rings of 2 μm. For proposed MZG-GR structure with S_1 = 1.3 μm, the maximum electric field is located at the middle rings and reduce to 2.5 MV/cm. It is also found that the simulated surface electric field distribution of the MZG-GR structure is more uniform than the conventional structure, thus avoiding early breakdown in the edge termination area. The MZG-GR structure, which forms a gradual decrease of effective charges in the junction termination region, optimizes the electric field profile and improves the robust of the device.

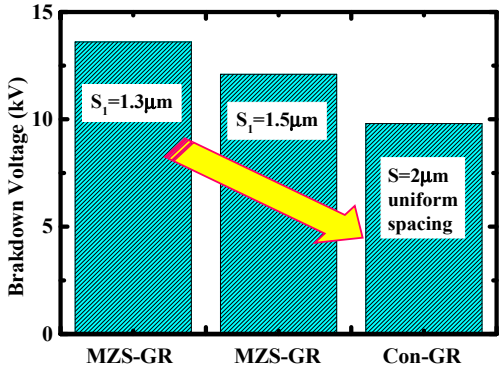

Figure 4. Measured reverse blocking characteristics for MZG-GR structure and the uniform spacing GR structure.

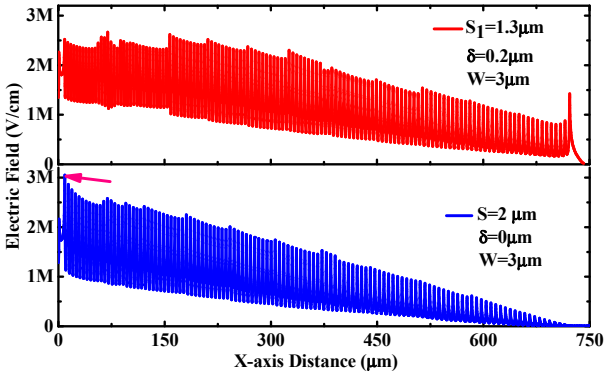

Fig. 5 Comparison of electric field distributions long the A-B cutline between the MSG-GR and conventional equally spaced GR structure at breakdown.

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3.2 On-State characteristics

On wafer forward I–V measurement are performed Forward characteristics of the fabricated SiC MOSFET transistors are measured on-wafer using a Cascade Microtech probe with IWATSU CT-3200 curve tracer. Typical forward I–V characteristics on both wafer are shown in Figure 6. The specific on-resistance ($R_{ON,SP}$) is 0.87 Ω.cm^2 at the room temperature for the SiC MOSFET with the active area of 3.2 mm^2. The high value of specific on-resistance is mainly attributed to the high drift region resistance without the application of the JFET implantation process.

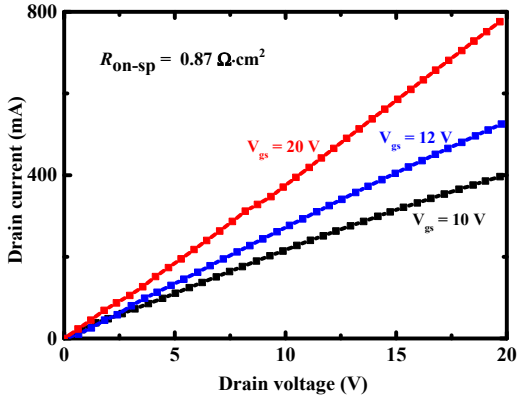

Figure 6. Measured on-state characteristics for SiC MOSFETs with MZG-GR structure.

4. Summary

In this paper, a multi-zone gradient guard ring technique have been employed in the ultrahigh voltage 4H-SiC power MOSFET for multi-gigawatt industry applications. The MZG forms a similar multiple-zone JTE technology, yielding the maximum breakdown voltage of 13.6 kV@10 μA with an area smaller than that of the equally spaced guard ring. The 2-D numerical device analyzed and experimental results shows that MZG-GR structure is an attractive candidates for ultra-high voltage switching applications.

Acknowledgments

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