2020 IEEE 15th International Conference on Solid-State and Integrated Circuit Technology

ICSICT-2020

Final Program

Nov. 3- Nov. 6, 2020, Kunming, China

2020 IEEE 15th International Conference on Solid-State and Integrated Circuit Technology

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Contents

Tutorials

09:00-10:30, Nov. 3, 2020

T-1 Electrostatic Discharge Design for Digital, Analog and Radio Frequency (RF) Applications

Dr. Steven Voldman , Comcast, USA

10:45-12:15, Nov. 3, 2020

T-2 CMOS Transceiver Realizing Terahertz Wireless Communication, The Key Technology of Beyond 5G

Prof. Minoru Fujishima, Graduate School of Advanced Sciences of Matter, Hiroshima University, Japan

14:00-15:30, Nov. 3, 2020

T-3 Fabrication and Applications of Bulk and SOI FinFETs

Dr. Rita Rooyackers ClaRoo, Leuven, Belgium

15:45-17:15, Nov. 3, 2020

T-4 Physical Hardware Attacks with Machine Learning

Prof. Bah-Hwee Gwee, NTU, Singapore

ICSICT 2020 Technical Program Overview

Date	Time	Room (A)	Room (B)	Room (C)	Room (D)	Room (E)
Nov.3	9:00:12:15	Tutorial Session T1 & T2				
	14:00-17:15	Tutorial Session T3 & T4				
Nov.4	8: 30-9: 00	Opening				
	9: 00-10: 30	Keynote Session K1-1 & K1-2				
	10: 45-12: 15	Keynote Session K2-1 & K2-2				
	13: 30-15: 30	Session A1	Session B1	Session C1	Session D1	Session E1
		SoC 1	Analog Circuit 1	Process technology	Device Technology	Focus session
	15: 45-17: 45	Session A2	Session B2	Session C2	Session D2	Session E2
		SoC 2	Analog Circuit 2	Process technology	Device Technology	Focus session
	17: 45-18: 45	Poster Session I device & process				
Nov.5	8: 30-10: 00	Keynote Session K3-1 & K3-2				
	10: 15-12: 15	Special Session A3	Session B3	Session C3	Session D3	Session E3
		AI Circuit & System 1	Analog Circuit 3	Compound & Organic devices	Device Technology	Special session
	13: 30-15: 30	Special Session A4	Session B4	Session C4	Session D4	Session E4
		AI Circuit & System 2	Analog Circuit 4	Compound & Organic devices	Photoelectron and TFT	Special session
Nov.5	15: 45-17: 45	Special Session A5	Session B5	Session C5	Session D5	Session E5
		Digital Circuit	RF Circuit 1	Photoelectron and TFT	Power Device and Reliability	AI and IoT (Process & Device)
	17: 45-18: 45	Poster Session II circuit design				
Nov.6	8: 30-10: 00	Panal Discussion Session Chair :				
	10: 15-12: 15	Session A6	Session B6	Session C6	Session D6	
		Clock Circuit	RF Circuit 2	Power Device and Reliability	Memory Technology	
	13: 30-15: 30	Session A7	Session B7	Session C7	Session D7	
		EDA 1	Data Converter 1	MEMS and Sensors	Memory Technology	
	15: 45-17: 45	Session A8	Session B8	Session C8	Session D8	
		EDA 2	Data Converter 2	Device Simulation and Modeling	Device Simulation and Modeling	
	17: 45-18: 45	Poster Session Ⅲ circuit design				

Paper Presentation Information

The 2020 IEEE ICSICT will have oral and poster sessions. All the papers included in the conference program should be presented in English by one of the authors at the arranged session.

1. Oral Presentation

Presentation time:

Invited paper (30 minutes): 30 min talk in video

Regular paper (15 minutes): 15 min talk in video

30min upload video is required.

2. Poster Presentation

Poster size: 120 cm (high) × 100 cm (wide)；5-10min talk in video

Poster Session 1:

Presentation time: 17:45-18:45 on Nov. 4, 2020.

Display time: 8:30-18:45 on Nov. 4, 2020.

Poster Session 2:

Presentation time: 17:45-18:45 on Nov. 5, 2020.

Display time: 8:30-18:45 on Nov. 5, 2020.

Poster Session 3:

Presentation time: 17:45-18:45 on Nov. 6, 2020.

Display time: 8:30-18:45 on Nov. 6, 2020.

Technical Sessions

Keynote Session 1

Session Chair: Prof. Ru Huang (Peking University, China)

09:00 Nov.4 **K1-1** (Invited)
Enabling 5G and EDGE AI advances in slowing Moore's Law era
Dr. Chidi Chidambaram
VP of Qualcomm, USA

09:45 Nov.4 **K1-2** (Invited)
Technology Innovations: DRAM, NAND & Emerging Memory
Dr. Jeongdong Choe
Senior Technical Fellow at TechInsights, Canada (Abstract)

Keynote Session 2

Session Chair: Prof. Wei Zhang (Fudan University, China)

10:45 Nov.4 **K2-1** (Invited)
Negative Capacitance in Ferroelectric-Gated MOSFETs: Is It Science Fact or Science Fiction?
Prof. T.P. Ma
Yale University, USA

11:30 Nov.4 **K2-2** (Invited)
Role of Implant and BASN Technologies in Enabling a Global-scale Deployment of Future Sensor-rich Telemedicine Paradigm
Prof. Habib F Rashvand
Warwick University, UK

Session A1 SOC 1(ROOM A)

Session Chair: Prof. J.F Kang (Peking University, China)

13:30 Nov.4 **A1-1** (Invited)
Feeding Computation Units As Needed
Yaohua Wang
School of Computer Science, National University of Defense Technology, Changsha, China

14:00 Nov.4 **A1-2** (Invited)
SPAD Properties and the Implications on Signal Processing for SPAD-based LiDARs
Tzu-Hsien Sang[1]*, TsungPo Yu[1], and Ning-Kai Yang[1]
[1]Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan

14:30 Nov.4 **A1-3**
HPME: A High-Performance Hardware Memory Encryption Engine Based on RISC-V TEE
Tianyu Yin[1], Guozhu Xin[1], Jun Han[1]
[1]State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

14:45 Nov.4 **A1-4**
Research and Development of QR Code Steganography Based on JSteg Algorithm in DCT Domain
Yanfei Sun[1], Mengyuan Yu[1], Junyu, Wang[1,2]*
[1]State Key Laboratory of ASIC&System, Fudan University, Shanghai, China; [2]Zhuhai Fudan Innovation Institute, Zhuhai Guangdong, China

15:00 Nov.4 **A1-5**
Multi-channel signal processing heterogeneous microsystem based on FPGA and Application Processor
Fan Chang, Jun Cheng, Jianling Yang, Hanting Huang, Kuizhi Mei*

School of Microelectronics, Xi'an Jiaotong University, Xi'an, China

15:15 Nov.4 **A1-6** **A Novel Shortest-distance Path-based Multicast Routing Algorithm for Network-on-Chips**

Yong Qin, Yi Liu*, Changqin Xu, Xiaodong Wen
Department of Microelectronics, Xidian University, Xian, China

Session B1 Analog Circuit 1(ROOM B)

Session Chair: Haruo Kobayashi (Gunma University,Japan)

13:30 Nov.4 **B1-1** (Invited) **High Voltage CMOS Bidirectional Current Sensor for Battery Monironing in Portable Devices**

Chua-Chin Wang[1], Pang-Yen Lou[1], Zong-You Hou[1], Hsiu-Chun Tsai[1], Yi-Jen Chiu[1], Yu-Cheng Lin[2]
[1]National Sun Yat-Sen Univ. Kaohsiung, Taiwan; [2]National Cheng Kung Univ. Tainan, Taiwan

14:00 Nov.4 **B1-2** **A wideband transimpedance amplifier with tee network topology**

Rui Yang, Shao-Wei Zhen*, You-Run Zhang, Yi-Qiang Zhao, Xiao Yang, Bo Zhang
School of Electronic Science and Engineering (National Exemplary School of Microelectronics), University of Electronic Science and Technology of China, Chengdu 610054, China; State key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

14:15 Nov.4 **B1-3** **A 1V Supply, 81nW, 800mv Bandgap Reference Voltage Circuit for Low Power Devices**

Peng Cao, Zhiliang Hong*
State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

14:30 Nov.4 **B1-4** **High Precision Voltage Monitoring Technology for Multi-cell Battery Management System**

Li-Qing, Guo-Zhong Jie*, Chen-Hao, He-Shuai
Department of Electronic Engineering, Xi'an University of Technology, Xi'an, Shanxi, China

14:45 Nov.4 **B1-5** **A Self-Clocked Digital Low-Dropout Regulator with Dual Bisection Method Tuning**

Tiantian Mao, Da Li, Libo Qian*
Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo, China

15:00 Nov.4 **B1-6** **Research on Low Power Constant Transconductance Rail-to-Rail Operational Amplifier Technology**

HE Shuai, GUO Zhongjie*, ZHENG Xiaoyi, CHEN Hao, LI Qing
Department of Electronics, School of Automation and Information Engineering, Xi'an University of Technology, Xi'an, China

15:15 Nov.4 **B1-7** **A Low-Power 16-Channel SiPM Readout Front-end with a Shared SAR ADC in 180 nm CMOS**

Yuxuan Tang[1] , Runxi Zhang[2], and Jinghong Chen[1]
[1]Department of Electrical and Computer Engineering, University of Houston, Houston, TX 77204, USA; [2]Institute of Microelectronic Circuits and Systems, East China Normal University, Shanghai, China

Session C1 Process Technology 1(ROOM C)

Session Chair: Dr. Qiang Wu (ICRD)

13:30 **C1-1** **3D Nanocarbon Interconnects**

Nov.4 (Invited)

Changjian Zhou[1] and Cary Y. Yang[2]
[1]School of Microelectronics, South China University of Technology, Guangzhou, China; [2]Center for Nanostructures, Santa Clara University, Santa Clara, CA, USA

14:00 **C1-2** **Studying the Reliability of Ge nFinFETs by the Normalized Input-referred Voltage Noise**

Nov.4 (Invited)

Duan Xie[1,2], Eddy Simoen[2]*, Hiroaki Arimura[2]
[1] School of Electronic Engineering School of Electronic Engineering, Xi'an University of Posts &Telecommunications, Xi'an, China; [2]imec, B-3001 Leuven, Belgium

14:30 **C1-3** **Interconnect Structures for Reducing Intra-Layer Metal-to-Metal Capacitances**

Nov.4 (Invited)

Clarissa Prawoto, Ying Xiao, and Mansun Chan*
Department of Electronic and Computer Engineering, the Hong Hong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong SAR, P. R. China

15:00 **C1-4** **Evaluation of Cu/Graphene Integration Schemes for Its Application on CMOS BEOL Interconnect**

Nov.4

Xiaoxu Kang*[1], Zhengxi Cheng[2], Qingyun Zuo[1], Weijun Wang[1], Ruoxi Shen[1], Xiaolan Zhong[1], Zhangfa Chen[1], Shoumian Chen[1], Yuhang Zhao[1]
[1]Process Technologies Department, Shanghai IC R&D Center, ICRD, Shanghai, China; [2]Key Laboratory of Infrared Materials and Detectors, Shanghai Institute of Technical Physics, Chinese Academy of Sciences, Shanghai, China

Session D1 Device Technology 1(ROOM D)

Session Chair: Prof. Cor Claeys (KU Leuven, Belgium)

13:30 **D1-1** **Advanced Spin Orbit Torque Magnetic Random Access Memory with Field-Free Switching Schemes**

Nov.4 (Invited)

Chao Wang[1, 2], Zhaohao Wang[1, 3, 4]*, Shouzhong Peng[1, 3, 4], Youguang Zhang1, 2, Weisheng Zhao[1, 3, 4]
[1]Fert Beijing Research Institute, Beihang University, Beijing, China; [2]School of Electronics and Information Engineering, Beihang University, Beijing, China; [3]School of Microelectronics, Beihang University, Beijing, China; [4]Beijing Advanced Innovation Center for Big Data and Brain Computing, Beihang University, Beijing, China

14:00 **D1-2** **Status and trends in nanoscale CMOS and Beyond-CMOS**

Nov.4 (Invited)

Francis Balestra
Univ. Grenoble Alpes, CNRS, Grenoble INP, IMEP-LAHC, 38000 Grenoble, France

14:30 **D1-3** **Cryogenic Characterization of Nano-scale Bulk FinFETs**

Nov.4

Lin-Jie Fan[12], Jin-Shun Bi[12]*, Xue Fan[3]*, Gao-Bo Xu[12], Yan-Nan Xu[12], Kai Xi[1], and Zhan-gang Zhang[4]
[1]Institute of Microelectronics, Chinese Academy of Sciences, Beijing; [2] University of Chinese Academy of Sciences, Beijing; [3]School of Electrical Engineering, Chengdu Technological University, Chengdu; [4]Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, China Electronic Product Reliability and Environmental Testing Research Institute, Guangzhou

14:45 **D1-4** **Unijunction Transistor on Silicon-On-Insulator Substrate**

Nov.4

YX. Chen[1], J. Liu[1], K. Xiao[1], A. Zaslavsky[2], S. Cristoloveanu[3], FY. Liu[4]*, BH. Li[4]*,B. Li[4] and J. Wan[1]*
[1] State key lab of ASIC and System, School of Information Science and Engineering, Fudan University, Shanghai, China; [2]Department of Physics and School of Engineering, Brown

University, Providence, RI 02912, USA; [3]IMEP-LAHC, INP-Grenoble/Minatec, CS 50257, Grenoble 38016, France; [4]Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China

15:00 Nov.4 **D1-5** **A Novel HSPICE Model for Dual-Threshold Independent-Gate TFET**
Zihao Zhang, Jianping Hu*
Faculty of Information Science and Technology, Ningbo University, Ningbo, China

15:15 Nov.4 **D1-6** **Impact of Process Variability on Threshold Voltage in JLAM-VSN-FET**
Hao-feng Jiang, Cong Li*, Jia-min Guo, Fei-chen Liu, Zeng-guang Guo, Yi-qi Zhuang
School of Microelectronics, Xidian University, Xi'an, China

Session E1 Focus session(ROOM E)

Session Chair: Prof. Feng Miao (Nanjing University, China)

13:30 Nov.4 **E1-1** (Invited) **Advanced nanoelectronic characterization of materials and devices by conductive atomic force microscopy**
Mario Lanza[1]*
[1]Institute of Functional Nano and Soft Materials (FUNSOM), Collaborative Innovation Center of Suzhou Nanoscience & Technology, Soochow University, Suzhou, China

14:00 Nov.4 **E1-2** (Invited) **Polarization-Sensitive Photodetectors based on 2D Layered Semiconductors**
Zhongming Wei
Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China

14:30 Nov.4 **E1-3** (Invited) **Ferroelectric Field Effect Transistor for Low Power Applications**
Q. Huang*, M. Yang, J. Luo, H. Wang, C. Chen and R. Huang
Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University, Beijing, National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Beijing, China

15:00 Nov.4 **E1-4** (Invited) **Transiently chaotic simulated annealing based on intrinsic nonlinearity of memristors for efficient solution of optimization problems**
Yuchao Yang
Peking University

Session A2 SoC 2(ROOM A)

Session Chair: Prof. Yaohua Wang (National University of Defense Technology, China)

15:30 Nov.4 **A2-1** (Invited) **Design of a Low Power and High Efficiency Integrated System for Accurate Measurement of Blood Pressure of Human Body**
Liubin Li, Song Ma, Feng Zou, Yuhua Cheng*
Shanghai Research Institute of Microelectronics (SHRIME), Peking University, Shanghai, China; School of Electronics Engineering and Computer Science, Peking University, Beijing, China; Haian Innovation Center of Integrated Circuit Technologies, Haian, China

16:00 Nov.4 **A2-2** **A New Design Approach of SoP and Its Design Flow**
Xiao-Dong Weng*, Yi Liu, Ling-Yi Fan, Yin-Tang Yang
School of Microelectronics, Xidian University, Xi'an, China

16:15 Nov.4 **A2-3** **A 0.3-V 10-nW Rail-To-Rail OTA with Bulk-Driven Low-Impedance Compensation for Energy-Scavenging IoT Sensors**
Siwan Dong[1]*, Yu Wang[2], Xingyuan Tong[1], Cong Liu[1], Yarong Wang[1]

[1]School of Electronic Engineering, Xi'an University of Posts and Telecommunications, Xi'an, China; [2]Department of Electrical Engineering, Wright State University, Dayton, OH 45435, USA

16:30 Nov.4 **A2-4** **An Improved Design of Hybrid Integrated Voltage Regulator Based on DLDO and SCVR**
Yuanchen Qu and Pingqiang Zhou
School of Information Science and Technology Shanghaitech University Shanghai, China

16:45 Nov.4 **A2-5** **Dual-Source Energy Harvester with MPPT Technology based on Double Stack Resonance**
Keke Wang, Xiudeng Wang, Yinshui Xia*
Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo, China

17:00 Nov.4 **A2-6** **Analysis and optimization for Coil Misalignment in wireless power transfer**
Yong Shi, Xiaohang Wang, Libo Qian*
Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo, China

17:15 Nov.4 **A2-7** **An Ultra-Low-Voltage Single-Phase Adaptive Pulse Latch with Redundant Toggling Elimination**
Yingna Huang and Hailong Jiao
School of Electronic and Computer Engineering, Peking University Shenzhen Graduate School, Shenzhen, China

Session B2 Analog Circuit 2(ROOM B)

Session Chair: Prof. Chua-Chin Wang (National Sun Yat-Sen University, Taiwan/China)

15:30 Nov.4 **B2-1** (Invited) **Analog/Mixed-Signal Circuit Testing Technologies in IoT Era**
Haruo Kobayashi[1]*, Anna Kuwana[1], Jianglin Wei[1], Yujie Zhao[1], Shogo Katayama[1], Tran Minh Tri1, Manato Hirai[1], Takayuki Nakatani[1], Kazumi Hatayama[1], Keno Sato[2], Takashi Ishida[2], Toshiyuki Okamoto[2], Tamotsu Ichikawa[2]
[1]Division of Electronics and Informatics, Gunma University, 1-5-1 Tenjin-cho Kiryu, 376-8515, Japan; [2]ROHM Semiconductor, 2-4-8 Shin-Yokohama, Mimato-Kita-Ku, Yokohama 222-8575, Japan

16:00 Nov.4 **B2-2** **A Two-ASIC Front-End for MEMS Accelerometers**
Min Qi[1, 2]*, Chun-feng Bai[3], Yang Wang[3], Dong-hai Qiao[1]
[1]Institute of Acoustics, Chinese Academy of Sciences, Beijing, 100190, China;[2]University of Chinese Academy of Sciences, Beijing, China; [3]Soochow University, Suzhou, China

16:15 Nov.4 **B2-3** **A 10mV Input, 93.6% Peak Efficiency Three-mode Boost Converter for Thermoelectric Energy Harvesting**
Yihe Xing[1], Lianxi Liu[1,2]*
[1]School of Microelectronics, Xidian University, Shaanxi 710071, China;[2] Shaanxi Key Lab of Integrated Circuits and Systems, Xidian University, Xi'an, China

16:30 Nov.4 **B2-4** **A Photovoltaic and Thermal Energy Combining Harvesting Interface Circuit with MPPT and Single Inductor**
Peichao Zhang[1], Lianxi Liu[1,2]*
[1]School of Microelectronics, Xidian University, Shaanxi, China; [2]Shaanxi Key Lab of Integrated Circuits and Systems, Xidian University, Xi'an, China

16:45 **B2-5** **A Zero-Crossing Detection Circuit for Energy Harvesting**

Nov.4

Zhang Zhang[1] Tang Zechen[1] Hu Wei[1] Xie Guangjun[1] Liu Gang[2] Cheng Xin[1]*
[1]School of Electronics Science and Applied Physics, Hefei University of Technology, Hefei, China; [2]School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai, China

17:00 **B2-6** **A PVT-Robust Transimpedance Amplifier for Ultra-Low Current Sensing**
Nov.4
Hua-ping Chen, Lei Zhang*, and Yan Wang
Institute of Microelectronics, Tsinghua University, Beijing, China

17:15 **B2-7** **A Right-Half-Plane Zero-Free Single-Inductor Dual-Output Boost Converter with 92.44% Peak efficiency and Fast Transient Response**
Nov.4
Zhiguo Tong, Peng Cao, Xueli Zhang, Zhiliang Hong*
State Key Laboratory of ASIC & System, Fudan University, Shanghai, China

Session C2 Process Technology 2(ROOM C)

Session Chair: Prof. Cary Yang (Santa Clara University, USA)

15:30 **C2-1** **The Evolution of Photolithography Technology, Process Standards, and Future Outlook**
Nov.4 (Invited)
Qiang Wu[1]*, Yanli Li, and Yuhang Zhao
[1]Shanghai IC R&D Center, 497 Gaosi Road, Zhangjiang Hi-Tech Park, Shanghai, PR China

16:00 **C2-2** **A brief review of source/drain engineering in CMOS technology and future outlook**
Nov.4 (Invited)
Yiqun Liu*[1], Qingqing Wu, Jianjun Zhu, Qiang Wu, and Shoumian Chen
[1]Shanghai IC R&D Center, 497 Gaosi Road, Zhangjiang Hi-Tech Park, Shanghai, PR China

16:30 **C2-3** **Low Bonding Temperature Development for High Throughput 3D Heterogeneous Integration Platform**
Nov.4 (Invited)
Han-Wen Hu, and Kuan-Neng Chen
Department of Electronics Engineering, National Chiao Tung University

17:00 **C2-4** **The Soft X-Ray Lithography Performance under Typical Single-digit nm Logic Design Rules, Including Stochastics and Defectivity**
Nov.4
Yanli Li[1]*, Qiang Wu[1], Shoumian Chen
[1]497 Gaosi Road, Shanghai IC R&D Center, Shanghai, China

17:15 **C2-5** **Wireless data and power transfer in 3-D integration**
Nov.4
Xiaohang Wang, Yong Shi, Libo Qian*
Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo, China

17:30 **C2-6** **Electromigration Reliability of a Complex through Silicon via Structure**
Nov.4
Mengrong Zhang*, Enming Shang, Hong Lin, Shaojian Hu
SHANGHAI IC R&D CENTER, 497 Gaosi Road,Zhangjiang Hi-Tech Park, Shanghai, China

Session D2 Device Technology 2(ROOM D)

Session Chair: Prof. Runsheng Wang (Peking University, China)

15:30 **D2-1** **Light-stimulated artificial synapse based on Schottky barrier modulated CVD MoS2 transistors**
Nov.4 (Invited)
Qianlan Hu and Yanqing Wu[1,2]*

[1]Institude of Microelectronics and Key Laboratory of Microelectronic Devices and Circuits (MOE), Peking University, Beijing, China; [2]Wuhan National High Magnetic Field Center and School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China

16:00 **D2-2** **Technology Impact on the Low Frequency Noise of Si and Si/SiGe Superlattice Input-Output FinFETs**

Nov.4 (Invited)

Cor Claeys[1]*, Geert Hellings[2], Hiroaki Arimura[2], Bertrand Parvais[2], Lars-Åke Ragnarsson[2], Harold Dekkers[2], Tom Schram[2], Dimitri Linten[2], Naoto Horiguchi[2], Eddy Simoen[2], Dimitri Boudier[3] and Bogdan Cretu[3]

[1]EE Dept., KU Leuven, Leuven, Belgium; [2]Imec, Leuven, Belgium; [3]ENSICAEN, UNICAEN, CNRS, GREYC, University of Caen, Caen, France

16:30 **D2-3** **A Graphene Base Transistor for Potential Terahertz Application**

Nov.4

Chi Liu[1], Wei Ma[1,2], Maolin Chen[1,2], Wencai Ren[1,2], Dongming Sun[1,2]*

[1]Shenyang National Laboratory for Materials Science, Institute of Metal Research, Chinese Academy of Sciences, 72 Wenhua Road, Shenyang, China; [2]School of Materials Science and Engineering, University of Science and Technology of China, 72 Wenhua Road, Shenyang, China

16:45 **D2-4** **A LUT-Based Model of Tri-input TFET**

Nov.4

Han-Ye Gao, Jian-Ping Hu*

Faculty of Engineering and Computer Science, Ningbo University, Ningbo, China

17:00 **D2-5** **Physical Insights into the Impact of Internal Metal Gate on the Subthreshold Behavior of NCFET Based on Domain Switching Dynamics**

Nov.4

Tianyue Fu, Qianqian Huang*, Liang Chen, Chang Su, Ru Huang*

Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University, Beijing, China

17:15 **D2-6** **Improved Device Performance of MoTe2 nanoribbon Transistors with Solution-processed Ternary HfAlOx High-k Dielectric**

Nov.4

Yuan Liu[1,2], Zijian Xie[1,2], Li Yang[1,2], Xiaokun Wen[1,2], Wenyu Lei[1,2], Haixin Chang[1,2], Wenfeng Zhang[1,2]*

[1]Center for Joining and Electronic Packaging, State Key Laboratory of Material Processing and Die & Mould Technology, School of Materials Science and Engineering, Huazhong University of Science and Technology, Wuhan, China; [2]Shenzhen R&D Center of Huazhong University of Science and Technology, Shenzhen, China

Session E2 Focus session(ROOM E)

Session Chair: Prof. Yuchao Yang (Peking University, China)

15:30 **E2-1** **2D materials for next-generation computing technologies**

Nov.4 (Invited)

Peng Zhou

Fudan University, China

16:00 **E2-2** **2D van der Waals Heterostructures for Emerging Device Applications**

Nov.4 (Invited)

Feng Miao

School of Physics, Nanjing University, Nanjing, China

16:30 **E2-3** **Material Searching and Design for Phase-Change Memory Devices**

Nov.4 (Invited)

Xian-Bin Li [1]*

[1]State Key Laboratory on Integrated Optoelectronics and College of Electronic Science and Engineering, Jilin University, Changchun, China

17:00 **E2-4** **Ultrathin dielectric integration and reliability for 2D semiconductors**

Nov.4 (Invited)

Xinran Wang

School of Electronic Science and Engineering, Nanjing University, China

Session Poster Session I device & process

Session Chair: Prof. Saisheng Xu (Fudan University, China)

17:45 **P1-1** **fT Improvement of RF CMOS Transistor in Circuit-Level by Layout Optimization**

Nov.4

Zhi-Jian Chen[1]*, Peng-Cheng Huang[1], Bin Li[1], Yu-Chen Wang[1], Xiao-Ling Lin[2], Hong Chen[1]

[1]School of Microelectronics, South China University of Technology Guangzhou, Guangdong, China; [2]Electronic Product Reliability and Environmental Testing Research Institute, Guangzhou, China

17:50 **P1-2** **Optimization of Ion Implanter Hardware for Metal Contamination Reduction**

Nov.4

Xiaoxu Kang*[1], Junyu Xie[2], Long Tian[2], Zhangfa Chen[1], Dong He[1], Xiaoyu Sheng[1], Xiaoqiang Zhou[1], Ruoxi Shen[1], Xiaolan Zhong[1], Shoumian Chen[1], Yuhang Zhao[1], Shanshan Liu[3], Limin Zhu[3], Hanwei Lu[3], Yun Xu[3], Bo Zhang[3]

[1]Process Technologies Department, Shanghai IC R&D Center, ICRD, Shanghai, China; [2]BEIJING ZHONGKEXIN ELECTRONICS EQUIPMENT CO., LTD, Beijing, China; [3]Shanghai Huahong Grace Semiconductor Manufacturing Corporation, Shanghai, China

17:55 **P1-3** **Design and Implementation of a Low-cost AES Coprocessor Based on eSTT-MRAM IP**

Nov.4

Xingjie Liu[1], Yong Chen[1], Kaiwen Lu[1], Dongsheng Liu[1]*, Bo Liu[2], Quming Jiang[3]

[1]School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, China; [2]Key Laboratory of Spintronics Materials, Devices and Systems of Zhejiang Province, Hangzhou, China; [3]Chutian Dragon Co., Ltd., Dongguan, China

18:00 **P1-4** **Design for Saddle-Fin Device Performance Boosting with Dual Work Function Gate Formation Word Line**

Nov.4

Xiang Liu[1]*, River Jiang[1], Ning Li[1], Hang Yang[1], Jongsung Jeon[1], Blacksmith Wu[1], and Mark Cao[1]

[1]Product Research and Development, ChangXin Memory Technologies, Inc., Hefei, China

18:05 **P1-5** **Graphene-based Quantum Dots: Fabrication and Properties**

Nov.4

Xuemin Yu, Zhongzheng Tian, Muchan Li, Dacheng Yu, Liming Ren, and Yunyi Fu*

Institute of Micro-/Nanoelectronics, Peking University, Beijing, China

18:10 **P1-6** **A Comparison Study of Velocity Saturation Models for Gate-all-around MOSFETs**

Nov.4

Haotian Zhong[1], Zhao Rong[1], Xiaoqing Huang[1], Yihan Chen[2], Lining Zhang[1], Xinnan Lin[1]*

[1]School of Electronic and Computer Engineering, Peking University, Shenzhen, China; [2]School of HSS, The Chinese University of Hong Kong (Shenzhen), Shenzhen, China

18:15 **P1-7** **Charge Detrapping on Gate Edge of AlGaNGaN HEMT Under Drain Stress**

Nov.4

Rongkang Niu, Tianjiao Dai, Xinxin Zhang, Kuanchang Chang*, Xinnan Lin*

The Shenzhen Key Lab of Advanced Electron Device and Integration, School of Electronic and computer Engineering, Peking University Shenzhen Graduate School, Shenzhen, China

18:20 **P1-8**

Nov.4

Low temperature electric field dependent mobility of the current oscillation regime in silicon junctionless nanowire transistor

Chong Yang[1,2], Wei-Hua Han[1,2]*, Jun-Dong Chen[1,2], Xiao-Di Zhang[1,2] and Yang-Yan Guo[1,2]

[1]Engineering Research Center of Semiconductor Integrated Technology, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China; [2]Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences, Beijing, China

18:25 **P1-9**

Nov.4

A Novel Self-Aligned Dopant-Segregated Schottky Tunnel-FET with Asymmetry Sidewall Based on Standard CMOS Technology

Yiqing Li[1,2], Qianqian Huang[2]*, Mengxuan Yang[2], Ting Li[2], Zhixuan Wang[2], Weihai Bu[3], Jin Kang[3], Wenbo Wang[3], Shengdong Zhang[1], and Ru Huang[2]*

[1]School of Electronic and Computer Engineering, Peking University, Shenzhen, China; [2]Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University, Beijing, China; [3]Semiconductor Technology Innovation Center (Beijing), Beijing, China

18:30 **P1-10**

Nov.4

Influence of the acceptor-type trap on the characteristic of the short-channel GaN MOS-HEMT

Yijun Shi*, Zhiwei Fu, Bin Yao, Si Chen, Yiqiang Chen, Bin Zhou, Yun Huang, Zhizhe Wang

The Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, China Electronic Product Reliability and Environmental Testing Research Institute, Guangzhou, China

18:35 **P1-11**

Nov.4

A Study on the Threshold Voltage Shift under Gate-pulse Stress in D-mode GaN MIS-HEMTs

Xinxin Zhang, Rongkang Niu, Zhangwei Huang, Tianjiao Dai, Kuan-Chang Chang*, Xinnan Lin*

The Shenzhen Key Lab of Advanced Electron Device and Integration, School of Electronic and computer Engineering, Peking University Shenzhen Graduate School, Shenzhen, China

18:40 **P1-12**

Nov.4

An Optoelectronic Chip with excellent orthogonality for Encoder Application

Yu-Song Mu[1], Ning Ding[1], Yan Ma[1], Yu-Chun Chang[1]*

[1]State Key Laboratory on Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun, China

18:45 **P1-13**

Nov.4

Fully Self-Aligned Homojunction Bottom-Gate Amorphous InGaZnO TFTs with Al Reacted Source/Drain Regions

Xiaoliang Zhou[1], Yang Shao[1], Huan Yang[1], Qingping Lin[1], Lei Lu[1], Yi Wang[2], Shengdong Zhang[1,2]*

[1]School of Electronic and Computer Engineering, Shenzhen Graduate School, Peking University, Shenzhen, China; [2]Institute of Microelectronics, Peking University, Beijing, China

18:50 **P1-14**

Nov.4

Sputtering-Deposited Hafnium Oxide Dielectric for High-Performance InGaZnO Thin Film Transistors

Meng Li[1], Jun-Chen Dong[2]*, Qi Li[2], De-Dong Han[2], Zhi-Nong Yu[1]*, Yi Wang[2], Xing Zhang[2]

[1]School of Optics and Photonics, Beijing Institute of Technology, Beijing, China; [2] Institute of Microelectronics, Peking University, Beijing, China

18:55 Nov.4 **P1-15**

Performance enhancement of ATZO TFTs by component control and post treatment

Zhuang Yi, Dedong Han*, Junchen Dong, Huijin Li, Dazhong Zhou, Xing Zhang, and Yi Wang*

Institute of Microelectronics, Peking University, Beijing, China

19:00 Nov.4 **P1-16**

Enhancing WLCSP Reliability through Stress Relief Methods

Xin-Rong Liu*, Ya-Wei Dai*, Yan-Yan Zhu, Meng-Meng Hu

Department of Product Engineering, Hisilicon Technologies Co., LTD

19:05 Nov.4 **P1-17**

Study of Silicon Controlled Rectifier Devices with Different Dimensions for ESD Protection

Yize Wang[1], Junmin He[1], Yi Hu[2], Yubo Wang[2], Yuan Wang[1]*

[1]Key Laboratory of Microelectronics Device and Circuits (MoE), Institute of Microelectronics, Peking University, Beijing, P. R. China; [2]Beijing Smart-Chip Microelectronics Technology Co., Ltd., Beijing, China

19:10 Nov.4 **P1-18**

Investigation on Premature Breakdown Mechanisms in AlGaN/GaN HEMTs by TCAD simulations

Lingyan Shen [1]*, Xinhong Cheng[1], Li Zheng[1], Qi Luo[1], Zhongjian Wang[1]

[1]State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, P.R. China

19:15 Nov.4 **P1-19**

A Simple and Efficient Fuse-Trimming Circuit for Analog Design

Xianjie Wan, Lin Zhang, Jia Liu*, Jun Liu, and Dongbing Fu

Chongqing GigaChip Technology Co. Ltd., No.24 Institute of China Electronics Technology Group (CETC), Chongqing, P.R.China

19:20 Nov.4 **P1-20**

Simulation Studies about the NON Spacer Effects on the DRAM Access Transistor Performance

Xiang Liu[1]*, Jongsung Jeon[1], Blacksmith Wu[1], and Mark Cao[1]

[1]Product Research and Development, ChangXin Memory Technologies, Inc., Hefei, China

19:25 Nov.4 **P1-21**

Correlations between Static Noise Margin and Single-Event-Upset Hardness for SRAM Cells

Zhong-Shan Zheng[1, 2, 3]*, Zhen-Tao Li1, Bo Li[1, 2], Jia-Jun Luo[1, 2], Zheng-Sheng Han[1, 2, 3], Xin-Yu Liu[1, 2, 3]

[1]Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China; [2]Key Laboratory of Silicon Device Technology, Chinese Academy of Sciences, Beijing, China; [3]School of Microelectronics, University of Chinese Academy of Sciences, Beijing, China

19:30 Nov.4 **P1-22**

A new depth information detection pixel based on lateral Photodiode

Hang Xu, Lin Chen, Hao Zhu, Qing-Qing Sun* and David Wei Zhang

Department of Microelectronics, Fudan University, Shanghai 200433, China

19:35 Nov.4 **P1-23**

A computationally efficient nonlinear dynamic model for cMUT based on COMSOL and MATLAB/Simulink

Yan Wang[1], Le-Ming He[1,2], Ziwei Li[1], Weijiang Xu[2], Junyan Ren[1]*

[1]State Key Laboratory of ASIC and System, Fudan University, Shanghai, China; [2]Université Polytechnique Hauts-de-France, CNRS, Université Lille, ISEN. Centrale Lille, UMR 8520-IEMN- Institut d'Électronique de Microélectronique et de Nanotechnologie, DOAE—Département d'Opto-Acousto-Électronique, F-59313 Valenciennes CEDEX 9, France

19:40 Nov.4 **P1-24**

Isopropanol swelling of polydimethylsiloxane for reducing gold nanoparticles to enhance photoacoustic transducer

Qing Wang[1], Xubo Wang[1], Shuren Song[1], Antoine Riaud[1]*, Jia Zhou[1]

[1]State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University, Shanghai, China

19:45 Nov.4 **P1-25**

Physical and Electrical Characterization of Doped Amorphous Silicon Resistor

Xiaolan Zhong*[1], Xiaoxu Kang[1], Ruoxi Shen[1]

[1]Process Technologies Department, Shanghai IC R&D Center, ICRD, Shanghai, China

19:50 Nov.4 **P1-26**

Design Technology Co-Optimization for 3 nm Gate-All-Around Nanosheet FETs

Meng Wang[1], Yabin Sun[1]*, Xiaojin Li[1], Yanling Shi[1], Shaojian Hu[2], Enming Shang[2], Shoumian Chen[2]

[1]Key Laboratory of Multidimensional Information Processing, Department of Electrical Engineering, East China Normal University, Shanghai, China; [2]Integrated Circuit Research and Development Center, Shanghai, China

19:55 Nov.4 **P1-27**

SPICE Modeling and Verification of Wafer-Scale MoS2 Transistors

Xi Wang, Shunli Ma*, Wenzhong Bao*, Junyan Ren*

[1]State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

20:00 Nov.4 **P1-28**

Influence of Gate-Drain Underlap Length on Germanium Gate-All-Around Tunneling Field-Effect-Transistors

Kai-Xiao Wei, Xiao-Jin Li*, Ya-Bin Sun, Yan-Ling Shi

Key Laboratory of Multidimensional Information Processing, Department of Electrical Engineering, East China Normal University, Shanghai, China

20:05 Nov.4 **P1-29**

Single Event Transient Pulses Fault Injection Model based on LET for Circuit-Level Simulation

Chang-Qing Xu*, Yi Liu, Xiao-Dong Weng, Zhi-Bing Li, Yin-Tang Yang

School of Microelectronics, Xidian University, Xi'an, China

20:10 Nov.4 **P1-30**

Charge Plasma-Based Junctionless FinFET for The Immune of Fin Sidewall Angle Variation

Bao-Liang Liu[1], Hung-Chih Chin[2], Haijun Lou[3], Kuan-Chang Chang[1]*, Xinnan Lin[1]**

[1]The Shenzhen Key Lab of Advanced Electron Device and Integration ECE, Peking University Shenzhen Graduate School, Shenzhen, P.R.China; [2]Semiconductor Manufacturing International (Shenzhen) Corporation, Shenzhen, P.R.China; [3]The Institute of Advanced Technology, Zhejiang University, Hangzhou, P.R.China

20:15 Nov.4 **P1-31**

Static and Dynamic Simulation Study on 15 kV 4H-SiC p-Channel IGBTs

Xiao-Li Tian[1]*, Wang Feng[1, 2], Yu Yang[1, 2], Xiao-Fei Lu[1], Jiang Lu[1], Yun Bai[1]

[1]Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China; [2]College of Microelectronics, University of Chinese Academy of Sciences, Beijing, China

20:20 **P1-32**

A Wafer Map Defect Pattern Classification Model Based on Deep Convolutional Neural Network

Nov.4

Dong-yang Du*, Zheng Shi

Institute of VLSI Design, Zhejiang University, Hangzhou, China

20:25 **P1-33** **An Adaptive Gate Current Modulator based on Fuzzy PID for Voltage Equalization in Series Connected IGBTs**

Nov.4

Jia-Li Wan[1], Ze-Hong Li *, Xiao Zeng, Min Ren, Wei Gao, Jin-Ping Zhang, Bo Zhang, Zhao-Ji Li

[1]The State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronics Science and Technology of China (UESTC), Chengdu, Sichuan/China

20:30 **P1-34** **Dense-Atrous U-Net with salient computing for Accurate Retina Vessel Segmentation**

Nov.4

Xiao-Min Li[1], Geng-Sheng Chen[1], Shu-Yang Wang[2]*

[1]State Key Laboratory of ASIC and System, Fudan University, No.825 Zhangheng Road, Shanghai, China; [2]Department of Pathology, School of Basic Medical Sciences, Fudan University, No.130 Dong' an Road, Shanghai, China

20:35 **P1-35** **A Novel Process Variation Model for Test Cost Reduction in Wafers with Addressable Monitoring Structures**

Nov.4

Gui-Feng Ren[1]*, Zheng Shi[1]

[1]Institute of VLSI Design, Zhejiang University, Hangzhou, China

Keynote Session 3

Session Chair: Prof. Jan Van der Spiegel (University of Pennsylvania, USA)

08:30 **K3-1** **Self-Interference Cancellation Circuits and System for Full Duplex Communication and Neutral Interface Applications**

Nov.5 (Invited)

Prof. Chris Rudell

University of Washington, USA

09:15 **K3-2** **Recent Advancement in Li-Fi System-on-Chip Design and Emerging Applications**

Nov.5 (Invited)

Prof. Patrick Yue, Director

HKUST-Qualcomm Optical Wireless Lab, Hong Kong University of Science & Technology

Special Session A3 AI Circuit & System 1(ROOM A)

Session Chair: Prof. Tzu-Hsien Sang (Inst of Electronics, NCTU, Taiwan/China)

10:00 **A3-1** **Small-world-based Structural Pruning for Efficient FPGA Inference of Deep Neural Networks**

Nov.5 (Invited)

Gokul Krishnan[1], Yufei Ma[2], Yu Cao[1]

[1]School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA; [2]School of Electronics Engineering and Computer Science, Peking University, Beijing, China

10:30 **A3-2** **Flash-based Digital In-memory Computing for Deep Neural Networks**

Nov.5 (Invited)

Runze Han, Yachen Xiang, Peng Huang, Jinfeng Kang*

Institue of Microelectronics, Peking University, Beijing, China

11:00 **A3-3** **HOTCAKE: Higher Order Tucker Articulated Kernels for Deeper CNN Compression**

Nov.5 (Invited)

Rui Lin[1]*, Ching-Yun Ko[2], Zhuolun He[3], Cong Chen[1], Yuan Cheng[4], Hao Yu[5], Graziano Chesi[1], Ngai Wong[1]

[1]Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam, Hong Kong; [2]Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, USA; [3]Department of Computer Science and Engineering, Chinese University of Hong Kong, Shatin, NT, Hong Kong; [4]Department of Micro/Nanoelectronics, Shanghai Jiao Tong University, Shanghai, China; [5]Department of Electrical and Electronic Engineering, Southern University of Science and Technology, China

11:30 **A3-4** **Deep Spiking Binary Neural Network for Digital Neuromorphic Hardware**

Nov.5

Zilin Wang, Kefei Liu, Xiaoxin Cui*, Yuan Wang*

Key Laboratory of Microelectronics Device and Circuits (MOE) Institute of Microelectronics, Peking University, Beijing, P. R. China

11:45 **A3-5** **MF-Conv: A Novel Convolutional Approach Using Bit-Resolution-based Weight Decomposition to Eliminate Multiplications for CNN Acceleration**

Nov.5

Chen Yang*, Xianxian Lv, Bowen Li, Shiquan Fan, Kuizhi Mei, Li Geng

School of Microelectronics, Xi'an Jiaotong University, Shaanxi, China

12:00 **A3-6** **A Deep learning Feature Fusion Algorithm based on Lensless Cell detection system**

Nov.5

Shuaijun Li[1], Li Dai[1]*, Jianwei Li[1], Chen Wang[1], Ningmei Yu[1]

[1]School of Automation and Information Engineering, Xi'an University of Technology, Xi'an, China

12:15 **A3-7** **Fall Detection Based on an Inertial Sensor and a Customized Artificial Neural Network Algorithm**

Nov.5

Wei Ma[1], Zhiming Xiao[1], Xiaosai Liu[1], Dongyang Tang[2], Weibo Hu[1]*

[1]ICSS-LAB (SZ), College of Electronic Information and Optical Engineering, Nankai University, TJ, China; [2]College of Engineering, Texas Tech University, Lubbock, TX, USA

Session B3 Analog Circuit 3(ROOM B)

Session Chair: Prof. Zhao Zhang (Graduate School of Advanced Sciences of Matter, Japan)

10:00 **B3-1** **A High-stability Fast-recovery Floating Power Rail Generation Circuit for High-Voltage Applications**

Nov.5 (Invited)

Zekun Zhou*, Jiani Wang, Zhengyang Jin, Bo Zhang

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, Sichuan, China

10:30 **B3-2** **A High Dynamic Range Pixel Circuit with High-voltage Protection for 128×128 Linear-mode APD Array**

Nov.5

Yuting Gu[1], Wengao Lu[1]*, Yuze Niu[1], Yacong Zhang[1]*, Zhongjian Chen[1]

[1]Key Laboratory of Microelectronic Devices and Circuits , Department of Microelectronics, Peking University

10:45 **B3-3** **A Segmented Mach-Zehnder Modulators Driver in 0.13 um SiGe BiCMOS with an Output Swing of 3 Vppd at 25 Gb/s**

Nov.5

Jun Huang*, Dezhi Xing, Shuai Tang, Fangyuan Ren, Yao Wang

United Microelectronics Center Co., Ltd, Chongqing, China

11:00 **B3-4** **A high-efficiency WPT system with dual-output and enhanced coupling efficiency**

Nov.5

Mingming Zhang[1], Xian Tang[1]*, and Wai Tung Ng[2]

[1]Shenzhen International Graduate School, Tsinghua University, Shenzhen, China; [2]Department of Electrical and Computer Engineering, University of Toronto, Toronto, Canada

11:15 **B3-5** **DESIGN OF SIXTH-ORDER PASSIVE QUADRATURE SIGNAL GENERATION NETWORK BASED ON POLYPHASE FILTER**

Nov.5

MinhTri Tran[1], Akemi Hatta[2], Anna Kuwana[3], and Haruo Kobayashi[4]

Division of Electronics and Informatics, Gunma University, Kiryu, Japan

11:30 **B3-6** **Novel CMOS Positive and Negative Voltage Mutual Conversion Circuits and Regulators**

Nov.5

Moufu Kong*, Bin Wang, BingKe Zhang, Ke Huang, Jiaxin Guo, Jiawei Xu

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu

11:45 **B3-7** **A Configurable Transceiver for Eddy Current Angular Displacement Sensor with Angle Error <0.8°**

Nov.5

Yating Zou, Xuankai Zhi, Junshang Li, Yajie Qin*

State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

Session C3 Compound & Organic devices 1(ROOM C)

Session Chair: Dr. Eddy Simoen (imec, Belgium)

10:00 **C3-1** **Materials and Defect Aspects of III-V and III-N Devices for High-Speed Analog/RF Applications**

Nov.5 (Invited)

Eddy Simoen[1]*, Po-Chun (Brent) Hsu[1,2], Hao Yu[1], Hongyue Wang[1,3], Ming Zhao[1], Kenichiro Takakura[1,4], Vamsi Putcha[1], Uthayasankaran Peralagu[1], Bertrand Parvais[1], Niamh Waldron[1], and Nadine Collaert[1]

[1]Imec, Kapeldreef 75, B-3001 Leuven, Belgium; [2]Depart of Materials Eng., KU Leuven, 3001 Leuven, Belgium; [3]Depart of Electronics Eng. And Computer Sci., Peking University, Beijing, China; [4]National College of Technology (KOSEN), Kumamoto-College, Kumamoto, Japan

10:30 **C3-2** **Defect Dehydrogenation in Si-MOS and Compound-Semiconductor- Based Devices**

Nov.5 (Invited)

D. M. Fleetwood[1,2],*, P. F. Wang[1], E. X. Zhang[1], R. D. Schrimpf[1], and S. T. Pantelides[2,1]

[1]Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashville, TN 37235, USA; [2]Department of Physics and Astronomy, Vanderbilt University, Nashville, TN 37235, USA

11:00 **C3-3** **Vertical GaN Power Transistor with Embedded Fin-shaped Diode for High Performance Power Conversion**

Nov.5

Tao Sun[1], Xiaorong Luo[1]*, Jie Wei[1], Dongfa Ouyang[1], Gaoqiang Deng[1], Siyu Deng[1], Qian Wang[2], Song Bo[2], Bo Zhang[1]

[1]State Key Laboratory of Electronic Thin Films and Integrated Devices University of Electronic Science and Technology of China, Chengdu, China; [2]State Key Laboratory of Wide-Bandgap Semiconductor Power Electronic Devices, Nanjing Electronic Devices Institute, Nanjing, China

11:15 **C3-4** **A Novel Ultra-thin-barrier AlGaN/GaN MIS-gated Hybrid Anode Diode Featuring**

Improved High-temperature Reverse Blocking Characteristic

Nov.5

Liyang Zhu[1], Qi Zhou[12]*, Kuangli Chen[1], Xiu Yang[1], Jiacheng Lei[3], Zhihua Luo[1], Chunhua Zhou[1], Kevin J. Chen[3], and Bo Zhang[1]
[1]University of Electronic Science and Technology of China (UESTC), Chengdu, China; [2]Institute of Electronic and Information Engineering of UESTC in Guangdong, Dongguan, China; [3]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Kowloon, Hong Kong

11:30 **C3-5** **A Low Input Capacitance p-GaN Gate HEMT with Split Source-Field-Plate for Low Switching Loss**

Nov.5

Fangzhou Wang, Wanjun Chen*, Xiaorui Xu, Yajie Xin, Yun Xia, Ruize Sun, Qi Zhou, Bo Zhang
State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China

Session D3 Device Technology 3(ROOM D)

Session Chair: Prof. Yanqing Wu (Peking University, China)

10:00 **D3-1** **Understanding Hot Carrier Degradation and Variation in FinFET Technology**

Nov.5 (Invited)

Runsheng Wang*, Zhuoqing Yu, Jiayang Zhang, Zixuan Sun, Zhe Zhang, Ru Huang
Institute of Microelectronics, Peking University, Beijing, China

10:30 **D3-2** **Reliability Challenges in Advanced Technology Node: from Transistor to Circuit**

Nov.5 (Invited)

Changze Liu*, Pengpeng Ren, Yongsheng Sun, Dan Gao, Weichun Luo, Zanfeng Chen and Yu Xia
Department of COT, Hisilicon Technologies Co., LTD, Shenzhen, China

11:00 **D3-3** **A 5 nm Logic FinFET Device Design**

Nov.5 (Invited)

Yu Ding[1]*, Xin Luo[1], Shaojian Hu[1], Qiang Wu[1], Shoumian Chen[1] and Yuhang Zhao[1]
[1]Shanghai Integrated Circuit Research and Development Center, No. 497 Gaosi Road, Pudong New Area, Shanghai, P. R. China

11:15 **D3-4** **Variation Investigation of Junction-less Transistor with Side-wall Charge-plasma Structure Induced by Line Edge Roughness**

Nov.5

Kai Liu[1], Hung-Chih Chin[2], Haijun Lou[3], Kuan-Chang Chang[1], Xinnan Lin[1]*
[1]The Key Laboratory of Integrated Microsystem, ECE, Peking University Shenzhen Graduate School, Shenzhen, P. R. China; [2]Semiconductor Manufacturing International (Shenzhen) Corporation, Shenzhen, P.R. China; [3]Research Center of MicroSatellite, Zhejiang University, Hangzhou, Zhejiang, China

11:30 **D3-5** **High-Frequency Performance of MoS2 Transistors at Cryogenic Temperatures**

Nov.5

Qingguo Gao[1,2], Chongfu Zhang[1,2]*, Zhenfeng Zhang[3], Zichuan Yi[2], Xinjian Pan[2], Feng Chi[2], Liming Liu[2], Xuefei Li[3], Yanqing Wu[3,4]*
[1]School of Information and Communication Engineering, University of Electronic Science and Technology of China, Chengdu, China; [2]School of Electronic Information, University of Electronic Science and Technology of China, Zhongshan Institute, Zhongshan, China; [3]Wuhan National High Magnetic Field Center and School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, China; [4]Institute of Microelectronics and Key Laboratory of Microelectronic Devices and Circuits (MOE) and Frontiers Science Center for Nano-optoelectronics, Peking University, Beijing, China

Session E3 Special session 1(ROOM E)

Session Chair: Prof. Jun Han (Fudan Univerity, China)

10:00 Nov.5 **E3-1** (Invited)

Design and Implementation of NFC Smart Card SoC with eSTT-MRAM IP

Kaiwen Lu[1], Xingjie Liu[1], Yong Chen[1], Dongsheng Liu[1]*, Bo Liu[2], Liang Wu[3]

[1]School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, China; [2]Key Laboratory of Spintronics Materials, Devices and Systems of Zhejiang Province, Hangzhou, China; [3]Chutian Dragon Co., Ltd., Dongguan, China

10:30 Nov.5 **E3-2** (Invited)

ESGAN: Edge Loss and Spatial Convolution Generative Adversarial Network for Image Inpainting

Liyu Lin[1], Yun Chen[1]*, GengSheng Chen[1], Xiaoyang Zeng[1]

[1]Department of Microelectronics, Fudan University, Shanghai, China

11:00 Nov.5 **E3-3** (Invited)

An Improved Synthesis Method of Logic Circuits based on the NMOS-like RRAM Gates

Wenqiang Ye, Xiaole Cui*, Ye Ma, Feng Wei

Key Lab of Integrated Microsystems Peking University Shenzhen Graduate School Shenzhen, China

11:30 Nov.5 **E3-4** (Invited)

Study on the hardening of single-event transient in D-type flip-flop based on InP HBT

Yutao Zhang*, Hongliang Lv, Yuming Zhang, Yimen Zhang, Xiaohong Zhao, Shaojun Li

The State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an, China

Special Session A4 AI Circuit & System 2(ROOM A)

Session Chair: Dr. Gokul Krishnan (Arizona State University, USA)

13:30 Nov.5 **A4-1** (Invited)

Low Power AI ASIC Design for Portable Edge Computing

Yuan Lei[1], Peng Luo[1], Chi Hong Chan[1], Xiao Huo[1], Yiu Kei Li[1], Mei Kei Ieong[1]*

[1]United Microelectronics Center (Hong Kong), Hong Kong SAR

14:00 Nov.5 **A4-2**

Hardware Implementation of Depthwise Separable Convolution Neural Network

Yancao Jiang[1], Jie Ren[1], Xiang Xie[1], Chun Zhang[1]*

[1]Institute of Microelectronics, Tsinghua University, Beijing, China

14:15 Nov.5 **A4-3**

A 681 GOPS/W~3.59 TOPS/W CNN Accelerator Based on Novel Data Flow Scheduling Scheme

Yan Li[1], Xiaoling Ding[1], Haichuan Yang[1], Xuan Zhang[1], Yu Gong[2], Bo Liu[2]*

[1]School of Integrated Circuits, Southeast University, Wuxi, China; [2]School of Electronic Science and Engineering, Southeast University, Nanjing, China

14:30 Nov.5 **A4-4**

A Lightweight CNN for Low-Complexity HEVC Intra Encoder

Xiaobo Guo, Qin Wang, Jianfei Jiang*

Department of Microelectronics and Nanoscience, Shanghai Jiaotong University, Shanghai, China

14:45 **A4-5**

Deep Compression Methods for Neural Network-based SAR-Pipelined ADC Calibrator

Nov.5

Chenhui Zhou[1], Min Chen[1], Ziwei Li[1], Chixiao Chen[2], Fan Ye[1] and Junyan Ren[1]*

[1]State-Key Laboratory of ASIC and System, Fudan University, Shanghai, China; [2]Academy of Engineering and Technologies, Fudan University, Shanghai, China

15:00 **A4-6** **Low Power Keyword Recognition Accelerator based on Approximate Calculation of Deep-Shift Neural Network**

Nov.5

Lepeng Huang[1], Zilong Zhang[2], Haichuan Yang[2], Yuhao Sun[2], Yu Gong[1], Wei Ge[1], Bo Liu[1]*

[1]School of Electronic Science and Engineering, Southeast University, Nanjing, China; [2]School of Integrated Circuits, Southeast University, Wuxi, China

15:15 **A4-7** **Hardware Trojan Attacks on the Reconfigurable Interconnections of Convolutional Neural Networks Accelerators**

Nov.5

Chen Yang*, Jia Hou, Minshun Wu, Kuizhi Mei, Li Geng

School of Microelectronics, Xi'an Jiaotong University, Xi'an, Shaanxi, China

Session B4 Analog Circuit 4(ROOM B)

Session Chair: Prof. Yuhua Cheng (Peking University, China)

13:30 **B4-1** **Ping-Pong Operated Inverter-based OTA using Correlated Level Shifting Technique**

Nov.5 (Invited)

Tianqiao Wu[1], Zhichao Tan[2], Ning Xie[3]*, Hao Zhang[4], and Le Ye[4]

[1]School of Electronics and Information Engineering, Anhui University, Hefei, China; [2]College of Information Science & Electronic Engineering, Zhejiang University, Hangzhou, China; [3]Shanghai Institute of Technology Physics, Chinese Academy of Sciences, Shanghai, China; [4]Information Technology Institute, Peking University, Tianjin Binhai, China

14:00 **B4-2** **A Low Power Voltage-Mode Driver Design for CIS Applications**

Nov.5 (Invited)

Zi-Rui Xiong

Department of Micro/Nano Electronics, Shanghai Jiao Tong University, Shanghai, China

14:30 **B4-3** **MEASUREMENTS OF SELF-LOOP FUNCTIONS IN HIGH-ORDER PASSIVE AND ACTIVE LOW-PASS FILTERS**

Nov.5

MinhTri Tran[1], Anna Kuwana[2], Haruo Kobayashi[3]

Division of Electronics and Informatics, Gunma University, Kiryu 376-8515, Japan

14:45 **B4-4** **DESIGN OF LC HARMONIC NOTCH FILTER FOR RIPPLE REDUCTION IN STEP-DOWN DC-DC BUCK CONVERTER**

Nov.5

MinhTri Tran[1], Yasunori Kobori[2], Anna Kuwana[3], Haruo Kobayashi[4]

Division of Electronics and Informatics, Gunma University, Kiryu 376-8515, Japan

15:00 **B4-5** **A Pixel Readout Circuit for Hybrid SDD and CMOS Technology**

Nov.5

Yongsheng Wang[1]*, Lei Li[1], Jinhong Duan[1], Yue Song[1], Fangfa Fu[1], Fengchang Lai[1]

[1]Department of Microelectronics, Harbin Institute of Technology, Heilongjiang, China

15:15 **B4-6** **Comprehensive Analysis of Crosstalk Effect at DDR Channel**

Nov.5

Maosong Ma*, Xinwang Chen, Jianbin Liu

System Application Engineering, Changxin Memory Technologies, Inc., Shanghai, China

Session C4 Compound & Organic devices 2(ROOM C)

Session Chair: Dr. Francis Balestra (IMEP-LAHC, France)

13:30 **C4-1** **Solution Printing of Hybrid Semiconductor Films for Electronic Applications**

Nov.5 (Invited)

Ming He

Department of Microelectronics, Peking University, Beijing, China

14:00 **C4-2** **From 5G to 6G: will compound semiconductors make the difference?**

Nov.5 (Invited)

N. Collaert*, A. Alian, A. Banerjee[1], V. Chauhan[1], R. Y. ElKashlan[2], B. Hsu[3], M. Ingels, A. Khaled, K. Vondkar Kodandarama, B. Kunert, Y. Mols, U. Peralagu, V. Putcha, R. Rodriguez, A. Sibaja-Hernandez, E. Simoen, A. Vais, A. Walke, L. Witters, S. Yadav, H. Yu, M. Zhao, P. Wambacq[2], B. Parvais[2] and N. Waldron

Imec, Kapeldreef 75, 3001 Heverlee, Belgium;[1]Imec, Kissimmee, Florida, USA; [2]Also with VUB, Brussels, Belgium; [3]Also KU Leuven, Leuven, Belgium

14:30 **C4-3** **Gate Reliability and V_{TH} Stability Investigations of *p*-GaN HEMTs**

Nov.5 (Invited)

Mengyuan Hua[1,]*, Chengcai Wang[1], Junting Chen[1], Li Zhang[2], Zheyang Zheng[2], and Kevin J. Chen[2]

[1]Department of Electrical and Electronic Engineering, The Southern University of Science and Technology, Shenzhen, China; [2]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Kowloon, Hong Kong, China

15:00 **C4-4** **A Novel GaN Junction Field-Effect Transistor with Intrinsic Reverse Conduction Capability**

Nov.5

Kuangli Chen[1], Qi Zhou[12]*, Liyang Zhu[1], Zhiwen Dong[1], Yonglian Cai[1], Chunhua Zhou[1], Wanjun Chen[1], and Bo Zhang[1]

[1]University of Electronic Science and Technology of China (UESTC), Chengdu, China; [2]Institute of Electronic and Information Engineering of UESTC in Guangdong, Dongguan, China

15:15 **C4-5** **Study on Gate Leakage and Trapping Effect in InAlN/GaN HEMTs**

Nov.5

Xingye Zhou, Yuanjie Lv*, Xin Tan, Hongyu Guo, Yanmin Guo, Zhihong Feng*, Shujun Cai*

National Key Laboratory of ASIC, Hebei Semiconductor Research Institute, Shijiazhuang, P. R. China

15:30 **C4-6** **Research on Short Circuit Robustness of Corrugated p-body 4H-SiC MOSFET**

Nov.5

Xiuxiu Gao [1]*, Chengzhan Li [2], Fang Qi [1], Xiaoping Dai [1]

[1]CORESING SEMICONDUCTOR TECHNOLOGY CO . LTD, Zhuzhou,China; [2]ZHUZHOU CRRC TIMES SEMICONDUCTOR CO . LTD, Zhuzhou,China

Session D4 Photoelectron and TFT 1(ROOM D)

Session Chair: Prof. Xiaona Zhu (Fudan University, China)

13:30 **D4-1** **Progress of Lead-Free Halide Perovskite X-ray Detectors**

Nov.5 (Invited)

Hainan Zhang[1], Guanhua Dun[2], Yancong Qiao[3], Dan Xie[4], Tian-Ling Ren[5]*

Institute of Microelectronics, Tsinghua University, Beijing, China

14:00 **D4-2** **Silicon nitride-stressor and quantum size engineering in Ge quantum-dot light**

emission and photoresponsivity

Nov.5 (Invited)

Po-Yu Hong, Yu-Hong Kuo, Jung-Tsung Yang, Horng-Chih Lin, and Pei-Wen Li*

Institute of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, 300

14:30 **D4-3** **Fabrication and Characterization of T-gate Poly-Si Thin-Film Transistors**

Nov.5 (Invited)

Yu-An Huang and Horng-Chih Lin*

Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan

15:00 **D4-4** **Two-bit Storage Recording Head Based on the Magnetic Thin Film Device**

Nov.5

Muchan Li, Zhongzheng Tian, Xuemin Yu, Dacheng Yu, Liming Ren, and Yunyi Fu*

Institute of Micro-/Nanoelectronics, Peking University, Beijing, China

15:15 **D4-5** **A novel SOI-based ridge waveguide SiGe Heterojunction Phototransistor**

Nov.5

Ce Bian[1], Hong-Yun Xie[1]*, Min Guo[1], Yin Sha[1], Yang Xiang[1], Xian-Cheng Liu[1], Wan-Rong Zhang[1]

[1]Faculty of Information Technology, Beijing University of Technology, Beijing, China

Session E4 Special session 2(ROOM E)

Session Chair: Prof. Xiaole Cui (Peking University, China)

13:30 **E4-1** **An Ultra-low-power High-precision Dynamic Gesture Recognition Coprocessor Based On RISC-V Architecture**

Nov.5 (Invited)

Yong-Liang Zhang, Wei-Zhen Wang, Qiang Li, Zhi-Yan Jia, Jun Han, Xiao-Yang Zeng, Xu Cheng

State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

14:00 **E4-2** **Robust Clock Tree Synthesis for Near-threshold-voltage Circuits Design**

Nov.5 (Invited)

Zhenyu Xu[1], Xiangnan Song[1], Zexin Qin[1], Xuexiang Wang[2]*

[1]School of Microelectronics, Southeast University, Wuxi, Jiangsu; [2]National ASIC System Engineering Research Center, School of Electronic Science & Engineering, Southeast University, Nanjing, China

14:30 **E4-3** **A Low-Complexity Timing Mismatch Calibration Method for Four-Channel Time-Interleaved ADCs Based on Cross Correlation**

Nov.5 (Invited)

Sujuan Liu*, Lin Zhao, Zhiyue Deng, Zhonghou Zhang

College of Microelectronics, Beijing University of Technology, Beijing, China

15:00 **E4-4** **A Temperature-Compensated Voltage Reference with High PSRR**

Nov.5 (Invited)

Zekun Zhou[1], Shilei Li[1], Jianwen Cao[1], Yue Shi[2]*, Bo Zhang[1]

[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, Sichuan, China; [2]College of Communication Engineering, Chengdu University of Information Technology, Chengdu, China

Special Session A5 Digital Circuit(ROOM A)

Session Chair: Prof. Bei Yu (The Chinese University of Hong Kong, Hong Kong SAR, China)

15:45 **A5-1** Nov.5

A Design of Four Dies Parallel NAND Flash Memory Controller Supporting Toggle and ONFI mode

Qin Huang[1], Zilin Wang [1], Wengao Lu[2]*

[1]School of Software and Microelectronics, Peking University, Beijing, P.R. China; [2]Key Laboratory of Microelectronic Devices and Circuits, Department of Microelectronics, Peking University, Beijing, P.R. China

16:00 **A5-2** Nov.5

Implementation of Convolutional Neural Network with Co-design of High-Level Synthesis and Verilog HDL

Hejie Yu, Jun Cheng, Xiangnan Zhang, Yuzhe Gao, Kuizhi Mei*

School of Microelectronics, Xi'an Jiaotong University, Xi'an, China

16:15 **A5-3** Nov.5

Power-Aware Timing Analysis for High-Speed Memory Interface

Feng (Dan) Lin*, Zengquan Wu, Kang Zhao

Shanghai Design Center, Changxin Memory Technologies, Inc., Shanghai, China

16:30 **A5-4** Nov.5

A low-Power SRAM with charge cycling based read and write assist scheme

Hanzun Zhang[1], Song Jia[2]*, Jiancheng Yang[1], Yuan Wang[2]

[1]Institute of Microelectronics, Peking University, Beijing, China; [2]Key Laboratory of Microelectronic Devices and Circuits, Peking University, Beijing, China

16:45 **A5-5** Nov.5

An SEU (Single-event Upset) Mitigation Strategy on Read-Write Separation SRAM Cell for Low Power Consumption

Ze-Xin Su[12], Bo Li[1]*, Xiao-Hui Su[1], Fan-Yu Liu[1], Zheng-Sheng Han[12], Xin-Yu Liu[12], Konstantin 0. Petrosyants[3], Igor A. Kharitonov[4]

[1]Key Laboratory of Silicon Device and Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China; [2]University of Chinese Academy of Sciences, Beijing, China; [3]Institute for Design Problems in Microelectronics of Russian Academy of Sciences (IPPM RAS); [4]National Research University Higher School of Economics

17:00 **A5-6** Nov.5

A 7T1C Nonvolatile SRAM Based on Ferroelectric H_fO_2 Capacitor for Ultralow Power Applications

Chao Liu[1,2], Qiao Wang[1], Jianguo Yang*[1,3], Pengfei Jiang[1], Qingting Ding[1], Yuling Zhao[1], Qing Luo[1], Hangbing Lv[1], Ming Liu[1]

[1]Key Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China; [2]School of Microelectronics, University of Science and Technology of China, Hefei, China; [3]Zhejiang Lab, Hangzhou, China

17:15 **A5-7** Nov.5

Non-volatile In Memory Dual-Row X(N)OR Operation with Write Back Circuit Based on 1T1C FeRAM

Wang Qiao[1], Yuling Zhao[1], Jianguo Yang*[1,3], Chao Liu[1,2], Pengfei Jiang[1], Qingting Ding[1], Tiancheng Gong[1], Qing Luo[1], Hangbing Lv[1], Ming Liu[1]

[1]Key Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China; [2]School of Microelectronics, University of Science and Technology of China, Hefei, China; [3]Zhejiang Lab, Hangzhou, China

17:30 **A5-8** Nov.5

Novel Self-timing Speculative Writing for Unreliable STT-MRAM

Meng-Di Zhang[1], Hao Cai*[1,2], Lirida Naviner[2]

[1]National ASIC System Engineering Center, Southeast University, Nanjing, China; [2]Télécom Paris, 19 place Marguerite Perey, Palaiseau, France

Session B5 RF Circuit 1(ROOM B)

Session Chair: Prof. Yun Chen (Fudan University, China)

15:45 Nov.5 **B5-1** (Invited)

A CMOS Ka-Band Wireless Transceiver for Future Non-Terrestrial 6G Networks

Atsushi Shirane*, Yun Wang, Kenichi Okada

Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo, Japan

16:15 Nov.5 **B5-2**

Analysis and Design of Broadband, Transformer Based Matching Network

Chen Xing[1], Guixiang Jin[1], Tong Li[1], Na Yan[1]*, Yong Chen[2], Yue Lin[2], Hongtao Xu[1,2]

[1]State Key Laboratory of ASIC & System, Fudan University, Shanghai, China; [2]ICLegend Micro Co., Ltd., Shanghai, China

16:30 Nov.5 **B5-3**

The Ultra-Wideband 0.5-15GHz LNA for Reconfigurable Receiver System in 28 nm CMOS

Zhen-Feng Hu, Ma-Liang Liu*, Rui-Xue Ding, Zhang-Ming Zhu, Yin-Tang Yang

School of Microelectronics, Xidian University, Xi'an, China; 2 Taibai Road, Xi'an, Shanxi Province, China

16:45 Nov.5 **B5-4**

A Ka-Band High-Gain and Wideband mmW Down-Conversion Mixer for 5G Communication Applications

Rongsheng Bao[1], Shengyu Rao[1], Chunqi Shi[1], Jinghong Chen[2]*, Guangsheng Chen[3], and Runxi Zhang[1]*

[1]Institute of Microelectronic Circuits and Systems, East China Normal University, Shanghai, China; [2]Department of Electrical and Computer Engineering, University of Houston, Houston, USA; [3]Shanghai Eastsoft Microelectronics Co. Ltd., Shanghai, China

Session C5 Photoelectron and TFT 2(ROOM C)

Session Chair: Dr. Nadine Collaert (imec, Belgium)

15:45 Nov.5 **C5-1** (Invited)

Monolithic Integration of Fluorinated Metal-Oxide Thin-Film Transistor and Hydrogenated Amorphous Silicon Photo-Diode

Man Wong*, Sisi Wang, Zhichao Zhou

Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

16:15 Nov.5 **C5-2** (Invited)

Reliability of Flexible LTPS TFTs under Dynamic Mechanical Stress

Bin Li, Xiangyuan Yin, Wei Jiang, Mingxiang Wang*

, Dongli Zhang, Huaisheng Wang

School of Electronic and Information Engineering, Soochow University, Suzhou, China

16:45 Nov.5 **C5-3**

A dual-gate IGZO Source-Gated transistor based on field modulation by TCAD simulation

Ni Li, Zhao Rong, Lining Zhang*, Min Zhang*

School of Electronic and Computer Engineering, Peking University, Shenzhen, China

Session D5 Power Device and Reliability 1(ROOM D)

Session Chair: Prof. Mario Lanza (Soochow University, China)

15:45 Nov.5 **D5-1** (Invited)

Defect loss and its physical processes

Jian Fu Zhang*, Meng Duan, Mehzabeen Mehedi, Kean Hong Tok, Zeliang Ye, Zhigang Ji, and Weidong Zhang
School of Engineering, Liverpool John Moores University, Liverpool L3 3AF, UK

16:15 Nov.5 **D5-2**

Research on Low Frequency Power Loss of IGBT

Xiao-Liang Chen[1, 2]*, Tian Chen[2], Zhong-Jian Qian[2], Feng Xu[2], Wei-Feng Sun[1]
[1]National ASIC System Engineering Research Center, School of Electronic Science & Engineering,Southeast University, Nanjing, P. R. China; [2]China Resources Microelectronics Co., Ltd, Wuxi, P. R. China

16:30 Nov.5 **D5-3**

A Novel SOI-LIGBT With Short-Circuit and Over-Current Self-Protection

Moufu Kong*, Jiaxin Guo, Bingke Zhang, Jiawei Xu, Ke Huang, Bin Wang
State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China

16:45 Nov.5 **D5-4**

An Improved SPICE Based Behavior Model for Non-Snapback TVS Devices with Ultra-low Turn-on Resistance

Yanlin Nie[1]*, Qiupei Huang[1], Jizhi Liu[1], Zhiwei Liu[1]
[1]University of Electronic Science and Technology of China, Chengdu, Sichuan Province, P.R. China

17:00 Nov.5 **D5-5**

Experimental and Theoretical Study on EMI Noise of Superjunction MOSFET with Different Pillar Doping

Min Ren [1]*, Qiao Guo[1], Xuefan Zhang[1], Qingying Lei[1], Xin Zhang[2], Songrong Wu[3], Wei Gao[1], Zehong Li[1], Bo Zhang[1]
[1]State key Laboratory of Electronic Thin Films and Integrated device, University of Electronic Science and Technology of China, Chengdu, Sichuan, P. R. China; [2]Wuxi China Resources Huajing Microelectronics Co. LTD, Wuxi, Jiangsu, P. R. China; [3]Key Laboratory of Magnetic Suspension Technology and Maglev Vehicle, Ministry of Education, Chengdu, Sichuan, China

17:15 Nov.5 **D5-6**

The Superjunction Device with Optimized Process Window of Breakdown Voltage

Min Ren[1]*, Lv-Qiang Li[1], Yaoyao Lan[1], Rong-yao Ma[2], Xin Zhang[2], Fang Zheng[2], Wei Gao[1], Ze-Hong Li[1], Bo Zhang[1]
[1]State key Laboratory of Electronic Thin Films and Integrated devices, University of Electronic Science and Technology of China, Chengdu, P. R. China; [2]China Resources Microelectronics Co. LTD, Wuxi, Jiangsu, P. R. China

17:30 Nov.5 **D5-7**

High Performance Termination of Power Devices with Multi-epi Method

Yu-Zhen Liu[1], Ze-Hong Li[1]*, Tao Yu[2], Lu-ping Li[1], Hong Li[2], Min Ren[1], Jin-ping Zhang[1], Wei Gao[1], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, Chengdu, China; [2]Wuxi China Resources Huajing Microelectronics Co., Ltd, Wuxi, China

17:45 Nov.5 **D5-8**

High Performance Carrier Stored Trench Bipolar Transistor with Shield Emitter Trench

Jinping Zhang[1,2]*, Pengjiao Wang[1], Rongrong Zhu[1], Xiang Xiao[1], Zehong Li[1], Bo Zhang[1]
[1]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; [2]Institute of Electronic and Information Engineering of UESTC in Guangdong, Dongguan, China

Session E5 AI and IoT (Process & Device)(ROOM E)

Session Chair: Ming Li (Peking University)

15:45 Nov.5 **E5-1** (Invited)

Memristive devices and arrays for neuromorphic computing

J. Joshua Yang

Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, CA, USA

16:15 Nov.5 **E5-2** (Invited)

Low dimensional materials and devices for neuromorphic computing

Qi Chen[1], Yue Zhou[1], Yangyang Chen[1], Boyi Dong[1], Hui Yang[1], Zijian Tang[1], Xinchen Deng[1], Kexin Chen[1], Fuwei Zhuge[2], Yuhui He[1]*

[1]School of Optical & Electronic Information, Huazhong University of Science & Technology, China; [2]School of Materials Science & Engineering, Huazhong University of Science & Technology, China

16:45 Nov.5 **E5-3** (Invited)

Impact of RTN and Variability on RRAM-Based Neural Network

P. Freitas, Z. Chai, *W. Zhang, J. F. Zhang, J. Marsland

Department of Electronics and Electrical Engineering, Liverpool John Moores University, Liverpool L3 3AF, UK

17:15 Nov.5 **E5-4** (Invited)

Ferroelectric Transistors for Synaptic Devices: Challenges and Prospects

Shimeng Yu*, Panni Wang, Xiaochen Peng, and Yandong Luo

Georgia Institute of Technology

Session Poster Session Ⅱ circuit design

Session Chair: Prof. Huihua Yu (Fudan University, China)

18:00 Nov.5 **P2-1**

An IOSGO-CFAR Algorithm based on Clutter Classification and Recognition

Lintao Li[1] , Jiangyi Shi[1]* , Yuanyuan Li[1]， Zhaowei Su[1]， Xuan Liu[1]

[1]School of Microelectronics, XiDian University, Xian, China

18:05 Nov.5 **P2-2**

An Integrated SoC for Image Processing in Space Flight Instruments

Xuan Liu[1] , Jiangyi Shi[1*], Zhaowei Su[1] , Lintao Li[1]

[1]School of Microelectronics, XiDian University, Xian, China

18:10 Nov.5 **P2-3**

Self-optimizing Two-layer Network-on-Chip Based on Dominant Network-Flow Adaption

Yue Duan*, Jianwei Yang*, Jun Han*, Xiaoyang Zeng*

*State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

18:15 Nov.5 **P2-4**

Single Image Super-Resolution Neural Network Using FrequencyDomain Information

Yi Zhang, Minge Jing*, Yibo Fan, Xiaoyang Zeng

State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

18:20 **P2-5**

A CRCLA Task Partition Algorithm Combining Genetic Algorithm and Clustering Based Partitioning Algorithm

Nov.5

Yulei Zhang[1]*, Jinfu Xu[1] , Wei Li[1] , Longmei Nan[2] , Tao Chen[1]

[1]Institution of Information Science and Technology, Zhengzhou 450001, China; [2]Fudan University, Shanghai, China

18:25 **P2-6**

Research on Secure JTAG Debugging Model Based on Schnorr Identity Authentication Protocol

Nov.5

Wang Kai[1]*, Li Wei[1] , Chen Tao[1] , Nan Longmei[2]

[1]Key Laboratory of Information Security, Information Engineering University, Zhengzhou 450001, China; [2]Department of Microelectronics, Fudan University, Shanghai, China

18:30 **P2-7**

Design and Implementation of Cryptographic Instruction Set

Nov.5

Mengni Bie [1]*, Wei Li[1] , Tao Chen[1] , Longmei Nan[2]

[1]Information Engineering University, Zhengzhou, China; [2]Department of Microelectronics, Fudan University, Shanghai, China

18:35 **P2-8**

An Enhanced Data Cache with In-Cache Processing Units for Convolutional Neural Network Accelerators

Nov.5

Yu-Chao Zhou, Mai Lei, Yong-Liang Zhang, Quan Zhang, Jun Han

State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

18:40 **P2-9**

IDLA: An Instruction-based Adaptive CNN Accelerator

Nov.5

Peng Gao[1], Zhize Huang[1], Hanchen Ye[2], Gengsheng Chen[1]*

[1]State Key Laboratory of ASIC and System, Fudan University, No.825 Zhangheng Road, Shanghai, China; [2]University of Illinois at Urbana-Champaign, 1308 W Main St, Urbana, Illinois 61801, US

18:45 **P2-10**

An FPGA Based Heterogeneous Accelerator for Single Shot MultiBox Detector (SSD)

Nov.5

Liang Cai[1] , Feng Dong[2] , Ke Chen[2] , Kehua Yu[2] , Wei Qu[2] , Jianfei Jiang[1] *

[1]Department of Microelectronics and Nanoscience, Shanghai Jiao Tong University, Shanghai, China; [2]Beijing iQIYI Science & Technology Co., Ltd., Shanghai, China

18:50 **P2-11**

28nm 4Mb 1T-1MTJ STT-MRAM Circuits with Ultra-low Power Read Scheme

Nov.5

Si Wen Zheng[1], Jin Shun Bi[1,2]*, Kai Xi[1,2]*, Bo Li[1,2]*

[1] University of Chinese Academy of Sciences, Beijing, China [2] Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China

18:55 **P2-12**

Novel Radiation Hardened Memory Cell Design for Nanometer Technology

Nov.5

Li-Yi Xiao[1]*, Hong-Chen Li[1] , Jie Li[1] , He Liu[1]

[1]Microelectronic center, Harbin Institute of Technology, Harbin, China

19:00 **P2-13**

Scheme of Hardware Trojans Isolation for Switch Chip Buffer

Nov.5

Xiang-yu Li, Li-ji Wu*, Xiang-min Zhang

[1]Institute of Microelectronics, Tsinghua University, Beijing, China

19:05 **P2-14**

A 16-bit Arithmetic Logic Unit Design by Using Gate Diffusion Input

Nov.5

Yihang Duanmu[1] , Jianguo Yang[2] , Jinbao Li[1] , Xiaoyong Xue[1]*, Minge Jing[1] , Xiaoyang Zeng[1]

[1]State Key Lab of ASIC and System, School of Microelectronics, Fudan University, 825 Zhangheng Rd, Shanghai, China; [2]Zhejiang Lab, Hangzhou, China

19:10 **P2-15**

A Pico-second Resolution Sensor of NTV DFF Timing Variation with Cancelling Errors

from PVT and RC Delay along Testing Path

Nov.5

Wang Wang, Shuming Cui, Yinyin Lin*

[1]ASIC and System State Key Laboratory, Fudan University, Shanghai

19:15 **P2-16** **A Novel In-MRAM Multiplier Using Toggle Spin Torques Switching**

Nov.5

Kang-Xiang Xiong, Hao Cai

National ASIC System Engineering Center, Southeast University, Nanjing, China

19:20 **P2-17** **A LPDDR4X Low Jitter Driver Scheme with High Speed**

Nov.5

Yinchuan Gu[1]*, Jake Jung[1] , Chris Eom[1] , Brian Lee[1] , Edwin Kim[1] , Kanyu Cao [1] , Yiming Zhu[1]

[1]Design Department CXMT, Hefei, China

19:25 **P2-18** **A 2-stage with 3-stack Comparator with Common Mode Range Extension Technique for Mobile DRAM Interface**

Nov.5

Tao Zhang[1]*, Jake Jung[1] , Chris Eom[1] , Brian Lee[1] , Edwin Kim[1] , Kanyu Cao[1] , Yiming Zhu[1]

[1]Design Department CXMT, Hefei, China

19:30 **P2-19** **OTA–C Filter Based on the Low Noise and HD3 Transconductance for ECG Detection**

Nov.5

Bo Lin[1] , Zhiqiang Gao*[1] , Hongjun Li[2] , Jing Xu[2]

[1]Microelectronics Center, Harbin Institute of Technology, Harbin, China; [2]The 13th research institute of China electronics technology corporation

19:35 **P2-20** **A Feedback Loop-based Timing Adaptive Corrected Circuit**

Nov.5

Jun Liu[1]*, Lin Zhang[2] , Yabo Ni[1] , Jia Liu[1] , Xianjie Wan[1] , Yi Ding[1] , Dongbing Fu[2]

[1]National Key Laboratory of Analog Integrated Circuits Chongqing, CHINA; [2]Sichuan Institute of Solid-State Circuits Chongqing, CHINA

19:40 **P2-21** **A low power readout circuit for CMOS image sensor**

Nov.5

Ming Chen [1] , Li Zhou [1] , Yang-Jun Yang [2] , Cheng-Bin Zhang [1] , Kun-Yu Wang [1] , Cen Gao [1] , Wen-Jing Xu [1] , Jie Chen [1]*

[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China; [2]ZunYi Normal University, Zunyi, China

19:45 **P2-22** **A Design of 16-bit High Speed DAC with Segmented R2R Load**

Nov.5

Jun Liu[1]*, Dan Ma[2] , Xianjie Wan[1] , Weidong Yang[1] , Dongbing Fu[2]

[1]National Key Laboratory of Analog Integrated Circuits Chongqing, CHINA; [2]Sichuan Institute of Solid-State Circuits Chongqing, CHINA

19:50 **P2-23** **A Low Noise Precision Operational Amplifier**

Nov.5

Cheng-He Wang[1] , Liang Guo[1] *, Yuan-Jie Zhou[1]

[1]Sichuan Institute of Solid-State Circuits, Chongqing, China

19:55 **P2-24** **An Impedance Calibration Method Based on Temperature and Process Monitor for LPDDR5 Interface**

Nov.5

Miao Bai, Xiaofei Wang, Jing Jin, Tingting Mo

Department of Micro/Nano Electronics, Shanghai Jiao Tong University, Shanghai, China.

20:00 **P2-25** **Highly Reconfigurable Performance Monitoring Unit on RISC-V**

Nov.5 Mai Lei, Tian-Yu Yin, Yu-Chao Zhou, Jun Han

State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

Panel Session

08:30 **Topics: We are entering the Artifical Integlligence Era. Besides the applications and mathematical algorithms which most of us have been hearing about, what major changes do you expect that the AI would bring to the device and design technology world?**

Nov.6 Mediator: Shaofeng Yu, Fudan University

Panelists: Yuchao Yang, Peking University

Shimeng Yu, Gerogia Tech

Eddy Simoen, IMEC

Haruo Kobayashi , Gunma University

Meikei Ieong, HK-UMC

Antony Fan, Synopsys

Session A6 Clock Circuit (ROOM A)

Session Chair: Prof. Yue Shi (University of Electronic Science and Technology of China, China)

10:00 **A6-1** **Design of High-Performance Phase-Locked Loop Using Hybrid Dual-Path Loop Architecture: an Overview (Invited Paper)**

Nov.6 (Invited) Zhao Zhang[1] and Nanjian Wu[2, 3]*

[1]Graduate School of Advanced Science and Technology, Hiroshima University; [2]State Key Laboratory of Superlattice and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences; [3]Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences.

10:30 **A6-2** **A Multi-band CMOS VCO Based on Triple-coil Inductors**

Nov.6 Peng-Fei Yu[1], Zhi-Jian Chen[1]*, Bin Li[1], Xiao-Ling Lin[2], Chang-Jian Zhou[1]*

[1]School of Microelectronics, South China University of Technology Guangzhou; [2]Electronic Product Reliability and Environmental Testing Research Institute.

10:45 **A6-3** **A Bandwidth Adjusted PLL for Fast Chirp FMCW Radar Application**

Nov.6 Yu Xue, Chao Yang, Xiaoming Liu, Jing Jin*

Center for Analog/RF Integrated Circuits (CARFIC), Department of Micro/Nano Electronics, Shanghai Jiao Tong University.

11:00 **A6-4** **An Extended Range Multi-Modulus Divider with Seamless Switching at Extended Division Boundary**

Nov.6 Wenzheng Wang, Chao Yang, Yuan Liu, Jing Jin*

Center for Analog/RF Integrated Circuits (CARFIC), Department of Micro/Nano Electronics, Shanghai Jiao Tong University.

11:15 **A6-5** **Design of a Dual-Band Injection Locked Frequency Tripler with Sixth-Order Transformer-Based LC Tank**

Nov.6 Xiaoyan Wan[1], Wei Luo[1], Na Yan [1.2]*, Yong Chen [2], Yue Lin[2], Hongtao Xu [1.2]

[1]State Key Laboratory of ASIC and System, Fudan University; [2]ICLegend Micro Co., Ltd; [3]ICLegend Micro Intelligent (Suzhou) Co., Ltd

11:30 **A6-6** **Timing-based and Balanced Register Clustering in Near-threshold Voltage Clock Tree Design**

Nov.6

Xuexiang Wang[1]*, Yongkang Dong[2], Jiangwei Liang[1], Hao Zhang[1]

[1]National ASIC System Engineering Research Center, School of Electronic Science & Engineering, Southeast University; [2]School of Software, Southeast University.

Session B6 RF Circuit 2 (ROOM B)

Session Chair: Prof. Atsushi Shirane (Tokyo Inst of Technology, Japan)

10:00 **B6-1** (Invited)
Nov.6

CMOS Transformer Design for X-band Power Amplifier Applications

Zhichao Li∗, Shiheng Yang†, Hang Liu∗ and Kiat Seng Yeo∗

∗Singapore University of Technology and Design; †University of Electronic Science and Technology of China.

10:30 **B6-2**
Nov.6

A Real-Time 2.4-GHz Doppler Radar System with All Functionalities on Board for Vital Signal Detection

Wei Ma[1], Zhiming Xiao[1], Dongyang Tang[2], Fei Liu[1], Weibo Hu[1]*

[1]ICSS-LAB (SZ), College of Electronic Information and Optical Engineering, Nankai University, TJ, 2College of Engineering, Texas Tech University

10:45 **B6-3**
Nov.6

Design of An Efficient Wideband Quadrature Generator for Multiple Receivers Based on Poly-Phase Filter

Wei Luo[1], Na Yan[1,]*, Yong Chen[2], Yue Lin[2], Hongtao Xu[1]

[1]State Key Laboratory of ASIC and System, Fudan University; [2]ICLegend Corporation, Shanghai.

11:00 **B6-4**
Nov.6

Design of a Wideband CMOS Digital Step Attenuator with High Accuracy and Low Phase Error

Chen-Chen Yang[1], Na Yan[1,]*, Tong Li[1] , Yong Chen[2, 3], Yue Lin[2, 3] , Hongtao Xu

[1]State Key Laboratory of ASIC and System, Fudan University; [2]ICLegend Corporation, Shanghai; [3]ICLegend Micro Intelligent (Suzhou) Co., Ltd

Session C6 Power Device and Reliability (ROOM C)

Session Chair: Prof. Jian Fu Zhang (Liverpool John Moores University, UK)

10:00 **C6-1** (Invited)
Nov.6

Technological Development in Pursuit of High-Performance Normally-off GaN-based HEMTs

Wei-Chih Cheng[1], Guangnan Zhou[1], Fanming Zeng[1], Yang Jiang[1], Lingli Jiang[1], Qing Wang[1,2]*, and Hongyu Yu[1,3,4]*

[1]School of Microelectronics, Southern University of Science and Technology; [2]Dongguan Institute of Opto-Electronics Peking University; [3]Engineering Research Center of Integrated Circuits for Next-Generation Communications, Ministry of Education; [4]Shenzhen Institute of Wide-bandgap Semiconductors.

10:30 **C6-2** (Invited)
Nov.6

Dynamic Vth in p-GaN Gate Power HEMTs and Its Impacts upon Power Switching Circuits

Jin Wei[1,2]*, Han Xu[2], Ruiliang Xie[2], and Kevin J. Chen[2]*

[1]Institute of Microelectronics, Peking University; [2]Dept. of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong

11:00 **C6-3**
Nov.6

Narrow Gate Trench Power MOSFETs with Stepped Field Plate and Polysilicon Bridge

Zhengkang Wang, Ming Qiao*, Ruidi Wang, Zhaoji Li, Bo Zhang

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China.

11:15 Nov.6 **C6-4**

Improvement of Failure Current in Modified Later Silicon-Controlled Rectifier Device with N-type Floating Region

Junmin He[1], Yize Wang[1], Yi Hu[2], Dunshan Yu[1], Yuan Wang[1]*

[1]Key Laboratory of Microelectronics Device and Circuits (MoE), Institute of Microelectronics, Peking University, Beijing Smart-Chip Microelectronics Technology Co., Ltd.

11:30 Nov.6 **C6-5**

A Novel SiC MOSFET with Embedded Unipolar Diode

Xiaojie Xu[1], Xiaochuan Deng[1]*, Yunpeng Xing[1], Yi Wen[1], Zhiqiang Li[2], Xu Li[1], Bo Zhang[1]

[1]School of Electronic Science and Engineering, University of Electronic Science and Technology of China; [2]Microsystem and Terahertz Research Center, China Academy of Engineering Physics.

11:45 Nov.6 **C6-6**

Investigation of Surge Current Reliability of 1200V Planar and Trench SiC MOSFET

Wei Huang[1], Xiaochuan Deng[1, 2]*, Xu Li[1,2], Yi Wen[1,2], Xuan Li[1], Zhiqiang Li[3], Bo Zhang[1]

[1]School of Electronic Science and Engineering, University of Electronic Science and Technology of China; [2]Institute of Electronic and Information Engineering in Guangdong, University of Electronic Science and Technology of China; [3]Microsystem and Terahertz Research Center, China Academy of Engineering Physics, Mianyang.

12:00 Nov.6 **C6-7**

A New Semi-SJMOS for Improving the Reverse Recovery Soft and Dynamic Avalanche of the Body Diode

Le Su[1]*, Cai-Lin Wang[2], Wu-Hua Yang[3]

Department of Electronic Engineering, Xi'an University of Technology, Xi'an Key Laboratory of Power Electronic Devices and High Efficiency Power Conversion.

Session D6 Memory Technology (ROOM D)

Session Chair: Prof. You Yin (Gunma University, Japan)

10:00 Nov.6 **D6-1** (Invited)

Low-voltage operation of high-density ferroelectric domain wall memory

An Quan Jiang[1]*, Jun Jiang[1], Chao Wang[1]

[1]School of Microelectronics, Fudan University.

10:30 Nov.6 **D6-2** (Invited)

Read Disturbs in Triple-Level-Cell (TLC) 3D Charge-trap (CT) NAND Flash Memory

Jiezhi Chen

School of Information Science and Engineering, Shandong University.

11:00 Nov.6 **D6-3**

SCMOS: Series-Connected Memristor-only Stateful Logic

Zhiwei Li[1]*, Xi Zhu[1], Nan Li[1] and Hongchang Long[1]

[1]College of Electronic Science and Technology, National University of Defense Technology.

11:15 Nov.6 **D6-4**

Electrokinetic analysis of measured memristive characteristics in nanochannel-based interfacial memristor

Ke-Xin Chen[1], Yue Zhou[1], Yao-Yao Fu[1], Yu-Hui He[1]* and Xiang-Shui Miao[1]*

[1]Wuhan National Laboratory for Optoelectronics, School of Optical and Electronic Information, Huazhong University of Science and Technology.

11:30 Nov.6 **D6-5**

A DTCO approach on DRAM bit line capacitance and sensing margin improvement

Qinghua Han*, Mengfeng Cai, Blacksmith Wu, Kanyu Cao

PRD Division, ChangXin Memory Tech. co., Hefei

11:45 Nov.6 **D6-6**

Comprehensive Investigations on Data Pattern Dependences in Charge-trap (CT) 3D NAND Flash Memory

Yachen Kong, Xueyang Peng, Fei Wang, Menghua Jia, Xuepeng Zhan, Yuan Li, Jiezhi Chen*

School of Information Science and Engineering, Shandong University.

12:00 Nov.6 **D6-7**

Memory Modeling with Dynamic Time Evolution Method for Neuromorphic Circuit Simulations

Xiaoqing Huang[1], Xuhui Chen[1], Huifang Hu[1], Haotian Zhong[1], Lining Zhang[1]*, Mansun Chan[2], Ru Huang[3]

[1]School of Electronic and Computer Engineering, Peking University; [2]HKUST Shenzhen Research Institute, Shenzhen; [3]Institute of Microelectronics, Peking University.

Session A7 EDA 1 (ROOM A)

Session Chair: Dr. Antony Fan (Synposys, USA)

13:30 Nov.6 **A7-1** (Invited)

An Input-Sensitive Dynamic Power Modeling Methodology for AI Chips in Black-Box Form

Linfeng Zheng, Hui Zhao, Wei Gao and Pingqiang Zhou

School of Information Science and Technology, ShanghaiTech University

14:00 Nov.6 **A7-2** (Invited)

Reinforcement Learning Driven Physical Synthesis

Zhuolun He, Lu Zhang, Peiyu Liao, Yuzhe Ma, Bei Yu

Department of Computer Science and Engineering The Chinese University of Hong Kong

14:30 Nov.6 **A7-3** (Invited)

Hybrid III-V/Si-CMOS PDK for Monolithic Heterogeneously-Integrated III-V/Si Technology Platforms

Siau Ben Chiah[1], Xing Zhou[1]*, Binit Syamal[1], Kenneth Eng Kian Lee[2], Cheng Yeow Ng2, Eugene A. Fitzgerald[2,3]

[1]School of Electrical and Electronic Engineering, Nanyang Technological University

15:00 Nov.6 **A7-4**

Complex Placement Region Handling Based on Electrostatic System Modeling

Yongyi Guo[1], Yingjie Wu[1], Zhipeng Huang[2] and Jianli Chen[2]

[1]College of Mathematics and Computer Science, Fuzhou University; [2]Center for Discrete Mathematics and Theoretical Computer Science, Fuzhou University.

15:15 Nov.6 **A7-5**

An Enhanced Heuristic Layer Assignment Method in Global Routing

Jin-Wei Chen[1], Zhi-Xiong Di[1]*, Jia-Jie Chen[2], Quan-Yuan Feng[1], Jiang-Yi Shi[3]

[1]The School of Information Science and Technology, Southwest Jiaotong University; [2]Shanghai Academy of Spaceflight Technology; [3]School of Microelectronics, XiDian University.

15:30 Nov.6 **A7-6**

Detailed Routing Short Violations Prediction Method Using Graph Convolutional Network

Xuan Chen[1], Zhi-Xiong Di[1]*, Wei Wu[1], Quan-Yuan Feng[1], Jiang-Yi Shi[2]

[1]The School of Information Science and Technology, Southwest Jiaotong University; [2]School of Microelectronics, XiDian University

Session B7 Data Converter 1 (ROOM B)

Session Chair: Prof. Sujuan Liu (Beijing University of Technology)

13:30 **B7-1** **A 14bits 1GSPS Pipelined-SAR ADC with digital background calibration**
Nov.6 (Invited)
Xizhu Peng, Zhuoqun Zhong, Na Wu, Ruogu Hua, Yuefeng, Li, Haoyu Zhuang and He Tang
University of electronic science and technology of China

14:00 **B7-2** **An Input Frequency Insensitive Minimalism SAR with Semi-Synchronous Logic for Time-Interleaving Applications**
Nov.6
Ning Ding[1], Yu-song Mu[1], Jia-qi Jiang[1], Hong-bo Zhang[1], Yu-chun Chang[1]*
[1]College of Electronic Science & Engineering, Jilin University.

14:15 **B7-3** **A 10-bit 200MS/s SAR ADC with reference buffer in 40nm CMOS**
Nov.6
Jingfu Chen[1], Xinpeng Xing[1]*, Zhanpeng Yang[1], Haigang Feng[1], Zhihua Wang[2]
[1]Tsinghua Shenzhen International Graduate School, Tsinghua University; [2]Institute of Microelectronics, Tsinghua University.

14:30 **B7-4** **A Split-Based Neural Network Calibrator for SAR-Pipelined ADC on FPGA**
Nov.6
Min Chen[1], Chenhui Zhou[1], Wenbin He[1], Fan Ye[1] and Junyan Ren[1]*
[1]State-key Laboratory of ASIC and System, Fudan University

14:45 **B7-5** **All-Digital Background Calibration for Time-Interleaved ADC Using Differential Fir Filter**
Nov.6
Jiang-Bo Wei, Ma-Liang Liu*, Zhang-Ming Zhu, Yin-Tang Yang
School of Microelectronics, Xidian University.

15:00 **B7-6** **All-Digital Calibration Technology Based on Sign Judgment for TIADC Timing Mismatch**
Nov.6
Chen Hongmei[1]*, Xiao Rui[2], Yin Yongsheng, Deng Honghui, Meng Xu
[1]Department of Microelectronics, Hefei University of Technology.

15:15 **B7-7** **Adaptive Nonlinear Mismatch Calibration Technique for TIADC Based on Memory Polynomial Model**
Nov.6
Sujuan Liu*, Zhonghou Zhang, Can Liang, Chunqi Qian
College of Microelectronics, Beijing University of Technology

Session C7 MEMS and Sensors (ROOM C)

Session Chair: Prof. Weidong Zhang (Liverpool John Moores University, UK)

13:30 **C7-1** **Highly-Sensitive FET-based Sensor via Heterogeneous Selective-Assembling Integration of Porphyrin and Silicon Nanowires**
Nov.6 (Invited)
Xiaokang Li[1], Bocheng Yu[1], Gong Chen[1] and Ming Li*[1,2]
[1]Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University; [2]Frontiers Science Center for Nano-optoelectronics, Peking University.

14:00 **C7-2** **A Micromachined Multimodal Probe Technology for Ischemia Muscle Monitoring**

Nov.6 (Invited) Y. T. Cheng[1]* and Y. S. Chen[2]

[1]Microsystems Integration Laboratory, Institute of Electronics Engineering, National Chiao Tung University, HsinChu, Taiwan; [2]Department of Cardiovascular Surgery, National Taiwan University Hospital, Taipei, Taiwan.

14:30 **C7-3** **Ultrafast pyroelectric infrared photodetector enabled with singlecrystal ferroelectric thin films: design and modeling**

Nov.6 Xiaoxi Zhao[1], Guoyuan Li[1], Changjian Zhou[1]*

[1]School of Microelectronics, South China University of Technology.

14:45 **C7-4** **GAS SENSING CMOS TRANSISTORS BASED ON SOI SUBSTRATE**

Nov.6 K. Xiao[1], J. Liu[1], X. Liu[1]and J. Wan[1]*

[1]State key lab of ASIC and System, School of Information Science and Engineering, Fudan University, Shanghai, China .

15:00 **C7-5** **A High Sensitivity Biosensor Based On Vertically Stacked Silicon Nanosheet-FET**

Nov.6 Fei-Chen Liu, Cong Li*, Jia-Min Guo, Hao-Feng Jiang, Hai-Long You, Yi-Qi Zhuang

School of Microelectronics, Xidian University.

15:15 **C7-6** **An Acceleration Technology in CMOS Image Sensor Readout Circuit**

Nov.6 Su-ChangXu, Guo-Zhongjie*,Li-Chen, Liu-Shen, Cao-Xitao, Han-Xiao

School of Automation and Information Engineering, Xi'an University of Technology.

Session D7 Memory Technology (ROOM D)

Session Chair: Prof. Jiang Anquan (Fudan University, China)

13:30 **D7-1** **Electric induced magnetization switching in all oxide structure and single metallic layer**

Nov.6 (Invited) Jingsheng Chen

Department of Materials Science and Engineering, National University of Singapore.

14:00 **D7-2** **Chalcogenides and their applications to advanced phase-change-devices toward future IoT era**

Nov.6 (Invited) You Yin*, Wataru Matsuhashi, Koji Niiyama, Dai Nishijo, and Keita Sawao

Division of Electronics and Informatics, Gunma University.

14:30 **D7-3** **Impacts of Lateral Charge Migration on Data Retention and Read Disturb in 3D Charge-trap NAND Flash Memory**

Nov.6 Xueyang Peng, Fei Wang, Yachen Kong, Menghua Jia, Xuepeng Zhan, Yuan Li, Jiezhi Chen*

School of Information Science and Engineering, Shandong University.

14:45 **D7-4** **Modified Dropout and Maxout based on the MNN for improving accuracy**

Nov.6 Chao Wang[1], Xiaojing Zha, Yinshui Xia*

Faculty of Electrical Engineering and Computer Science, Ningbo University.

15:00 **D7-5** **Impact of back-gate bias on single event upset in monolithic 3-D integrated 6T SRAM based on a 22 nm FD-SOI technology**

Nov.6 Jun-Jun Zhang[1,2,3], Fan-Yu Liu[1,3]*, Bo Li[1,3], Yang Huang[1,2,3], Jin-Xing Cheng[4], Ying Gao[4], Can Yang[1,3], Xiao-Hui Su[1,3], Guo-Qing Wang[1,3], Jia-Jun Luo[1,3] and Zheng-Sheng Han[1,3]

[1]Institute of Microelectronics, Chinese Academy of Sciences; [2]University of Chinese Academy of Sciences; [3]Key Laboratory of Silicon Device and Technology, Chinese Academy of Sciences; [4]Beijing High Technique Institute.

15:15 Nov.6 **D7-6** **A Novel Page-Forming Scheme with Ultra-Low Bit-Error-Rate and High Reliability on a 1Mb RRAM Chip**

Junyi Wang[1], Liyang Pan[1,2,*], Bin Gao[1,2,*], Dabin Wu[1], Jianshi Tang[1,2], Huaqiang Wu[1,2,*], He Qian[1,2]

[1]Institute of Microelectronics, Beijing Innovation Center for Future Chips (ICFC), Tsinghua University; [2]Beijing National Research Center for Information Science and Technology, Tsinghua University.

15:30 Nov.6 **D7-7** **A Novel Neural Network with Digital Synaptic Weights Based on 3D NAND Flash Array**

Xinhe Wang, Bin Gao*, Jianshi Tang, He Qian

Institute of Microelectronics, Beijing Innovation Center for Future Chips (ICFC), Tsinghua University.

Session A8 EDA 2 (ROOM A)

Session Chair: Prof. Xing Zhou (Nanyang Technological University, Singapore)

15:45 Nov.6 (Invited) **A8-1** **Deflated Restarting of Exponential Integrator Method for Efficient Transient Circuit Simulation**

Meng Zhang, Jiaxin Li, Quan Chen

[1]Southern University of Science and Technology; [2]Southern University of Science and Technology; [3]Southern University of Science and Technology.

16:15 Nov.6 (Invited) **A8-2** **Advanced Circuit Verification for Robust Design**

Antony Fan, Joddy Wang, Vladimir Aptekar

Analog and Mixed-Signal Simulation Synopsys Inc.

16:45 Nov.6 **A8-3** **A Novel LUT Model for FET with Three-input Terminals**

Kai Dai, Jian-Ping Hu*, Ze-Qi Chen

Faculty of Electrical Engineering and Computer Science, Ningbo University.

17:00 Nov.6 **A8-4** **A Statistical Analysis Method for Reliability Data of Aerospace Components Based on Association Rules**

Chengzhi Jiang*, Xiaoming Fan

China Academy of Space Technology.

17:15 Nov.6 **A8-5** **Automatic design of analog integrated circuit based on multi-objective optimization**

Wei Mao, Jia-Hao Wei, Jing Wan*

State key lab of ASIC and System, School of Information Science and Engineering, Fudan University.

17:30 Nov.6 **A8-6** **New Bidirectional Fast BDD Dynamic Reordering Algorithm**

Juntao Li[1], Yang Yang[1], Guanting Huo[1], Guoyong Huang[2], Yufeng Jin*[1]

[1]Peking University Shenzhen Graduate School; [2]SMIT Group Limited, Shenzhen.

17:45 Nov.6 **A8-7** **Improved Hierarchical IR Drop Analysis in Homogeneous Circuits**

Chengrui Zhang and Pingqiang Zhou

Session B8 Data Converter 2 (ROOM B)

Session Chair: Fan Ye (Fudan University, China)

15:45 Nov.6 **B8-1**

A High Linearity T&H circuit for 1GHz Pipeline ADC in 65nm CMOS

H.J. Wu[1], Y. P. Zeng[2], X. L. Xing[1], N. Lin[1], and Q. Li[3*]

[1]Fudan Microelectronics Co., Ltd, Shanghai, China; [2]No.58, China Electronic Technology Group Corporation, Wuxi, China; [3]Shanghai Fudan Mircoelectronic Co.Ltd

16:00 Nov.6 **B8-2**

A VCO-Based Continuous Time Delta-sigma ADC with An Alternative Feedforward Scheme VCO

Mengying Hu, Yuekang Guo, Jing Jin*

Center for Analog/RF Integrated Circuits (CARFIC), Department of Micro/Nano Electronics, Shanghai Jiao Tong University

16:15 Nov.6 **B8-3**

A 10-bit 60MHz-BW Continuous-Time Delta-Sigma ADC for wireless applications in 40nm CMOS

Ze Wang[1], Xinpeng Xing[1]*, Xueqian Shang[1], Yi Ke[2] and Zhihua Wang[1]

[1]Tsinghua Shenzhen International Graduate School; [2]Silicon Integrated Co. Ltd

16:30 Nov.6 **B8-4**

A Fast Settling Low Noise Ring Amplifier for High Speed Pipelined SAR ADCs

Longbo Fan, Bingbing Ma, Na Yan*, Yun Yin, Hongtao Xu

State Key Laboratory of ASIC & System, Fudan University.

16:45 Nov.6 **B8-5**

A Multi-Channel 12 bit, 100Ksps 0.35um CMOS ADC IP core for Security SoC

Byambajav Ragchaa[1], Liji Wu[1]*, Xiangmin Zhang[2], Honghao Chu[3]

[2]Tsinghua National Laboratory for Information Science and Technology; Institute of Microelectronics, Tsinghua University

17:00 Nov.6 **B8-6**

Design of The Delta-Sigma Digital-to-Analog Converter For High-Resolution Micro-Nano Satellite Applications

Zhiqiang Gao[1]*, Bo Luan[1], Shuai Lin[1], Tengfei Li[1], and Jing Xu[2]*

[1]Department of Microelectronics, Harbin Institute of Technology, Harbin, China; [2]The 13th research institute of China electronics technology corporation, Shijiazhuang, China

17:15 Nov.6 **B8-7**

A Digital Synthesizable Full Common-mode Input Range Dynamic Voltage Comparator

Min Li*, Jue Wang, Xu Cheng, Jun Han, Xiaoyang Zeng

State Key Laboratory of ASIC and System, Fudan University

Session C8 Device Simulation and Modeling (ROOM C)

Session Chair: Xiaoyan Liu (Peking U)

15:45 Nov.6 (Invited) **C8-1**

New Method for Variability and Reliability-aware Device-Circuit Co-Design

Xiaoyan Liu[1,2] *, Wangyong Chen, LinLin Cai, Gang Du, Xing Zhang

[1]Institute of Microelectronics, Peking University, Beijing, China; [2]Beijing Engineering Research Center of Active Matrix Display, China

16:15 **C8-2** **Impacts of Poly-Si Channel on Cell Variations in Vertical Scaled Charge-trap (CT) 3D NAND Flash Memory**

Nov.6

Fei Wang, Xuepeng Zhan, Yuan Li, Jiezhi Chen*

School of Information Science and Engineering (ISE), Shandong University.

16:30 **C8-3** **Mathematic and Numerical analysis of Droplet-based Electricity Generator**

Nov.6

Cui Wang[1], Antoine Riaud[1]*

[1]Department of Microelectronics, Fudan University.

16:45 **C8-4** **A Novel High-Performance Bipolar GaN Diode Realized by Broadened Quantum Well and Three-Dimensional Carrier Sea**

Nov.6

Zeheng Wang, Chao Chen, Shengji Wang, Liang Li, Yuanzhe Yao*

School of Information and Software Engineering, University of Electronic Science and Technology of China.

17:00 **C8-5** **A Novel Enhancement-Type GaN HEMT with High Power Transmission Capability Using Extended Quantum Well Channel**

Nov.6

Zeheng Wang, Chengyu Che, Shengji Wang, Chao Chen, Zirui Wang, Yuanzhe Yao*

School of Information and Software Engineering, University of Electronic Science and Technology of China.

17:15 **C8-6** **Evaluation of Total Ionizing Dose Induced SER Variation Using Novel Transistor Degradation Model**

Nov.6

Jin-Jin Shao[1], Rui-Qiang Song[1]*, Xiao-Yu Zhang[1]

College of Computer, National University of Defense Technology.

17:30 **C8-7** **An Ultra-Low Gate Charge Shield Gate MOSFET with Pinch-Off Region and Schottky Contact**

Nov.6

Ruidi Wang, Wenyang Bai, Ming Qiao*, Zhixuan Li, Zhengkang Wang, Bo Zhang

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China.

Session D8 Device Simulation and Modeling (ROOM D)

Session Chair: Dr. Rui Yin (National IC Innviation Center, China)

15:45 **D8-1** **Electrothermal Model Parameters Extraction and Evaluation Based on BSIM-CMG for 7-nm Nanosheet Gate-All-Around Transistor**

Nov.6

Ren-Hua Liu, Si-Qi Yang, Xiao-Jin Li*, Ya-Bin Sun, Yan-Ling Shi

Shanghai Key Laboratory of Multidimensional Information Processing and the Department of Electrical Engineering, East China Normal University

16:00 **D8-2** **An Efficient PWL Memristor Model Towards Circuit Design**

Nov.6

Yufei Zhang, Zhiwei Li, Changlin Chen*

College of Electronic Science and Technology, National University of Defense Technology.

16:15 **D8-3** **Characterization Simulation of a Bulk MOSFET in Steady-State with SIPG Method**

Nov.6

Jun-Yan Zhu[13], Chen Song[2]*, Vincent Heuveline[2],Bo Li[1], Bin-Hong Li[1], Zheng-Sheng Han[13]**, Xin-Yu Liu[13]

[1]Institute of Microelectronics of the Chinese Academy of Sciences; [2]Heidelberg University; [3]University of Chinese Academy of Sciences.

16:30 Nov.6 **D8-4** **RC Tightened Corner Test structure Design and Silicon Characterization in FinFET Technology**

Lijie Sun[1]*, Zhen Zhou[2], Mengying Zhang[1], Guangxing Wan[1], Waisum Wong[1], Xiaojin Li[2], Yabin Sun[2], Yanling Shi[2]

[1]Department of COT Design, Hisilicon Corporation, Shanghai; [2]School of Communication& Electronic Engineering, East China Normal University.

16:45 Nov.6 **D8-5** **Switching characteristics and simulated iodine vacancies distribution of halide perovskite RRAM**

Yu-Han Sun,[1] Yang Huang,[1] Ling-Zhi Tang,[1] Chen Wang,[1]*

[1]School of Microelectronics, Dalian University of Technology.

17:00 Nov.6 **D8-6** **RF GaN Device Model Survey and Model Parameter Extraction Flows**

Raj Sodhi, Roberto Tinti, Mark Dunn, Ma Long*

PathWave Design Solutions (PSS), Keysight Technologies Inc.

Session Poster Session Ⅲ circuit design

Session Chair: Prof. Ngai Wong (The University of Hong Kong, Hong Kong SAR/China)

18:00 Nov.6 **P3-1** **A 100MS/s Linear Gain-Boosted Capacitively Degenerated Dynamic Amplifier for Pipelined ADCs**

Ziwei Li, Wenbin He, Yan Wang, Fan Ye* and Junyan Ren

State Key Laboratory of ASIC and System Fudan University, Shanghai, China

18:05 Nov.6 **P3-2** **An Energy-Efficient Dynamic Comparator with Push-Pull Cross-Coupled Pre-Amplifier for SAR ADCs**

Ziwei Li, Wenbin He, Chenhui Zhou, Fan Ye* and Junyan Ren

State Key Laboratory of ASIC and System Fudan University, Shanghai, China

18:10 Nov.6 **P3-3** **A CMOS Readout Circuit with Low Detection Limit and High Linearity for Perovskite-based Direct X-ray Detector**

Hao Li[1] , Guang-Da Niu[1,2] , Zheng Nie[1] , Jiang Tang[1,2] , Dong-Sheng Liu[1,2]*

[1]School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, China; [2]Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan, China

18:15 Nov.6 **P3-4** **A Low-Pass Sense and Control Circuit for Switching Amplifier in Wideband Hybrid Envelope Tracking Supply Modulator**

Xueli Zhang, Peng Xu, Zhiliang Hong*

State Key Laboratory of ASIC & System, Fudan University, Shanghai, China

18:20 Nov.6 **P3-5** **A 187-pW 51-ppm/℃ Self-Adjusting Voltage Reference Circuit**

Mingwei Zhu[1,2] , Kaixuan Du[1,2,] Tianqiao Wu[1,2], Changwu Song[1,2] and Le Ye[2,3]*

[1]School of Electronics and Information Engineering, Anhui University, Hefei, 230601, China; [2]Key Laboratory of Microelectronic Devices and Circuits (MOE)Institute of Microelectronics, Peking university, Beijing, China; [3]Information Technology Institute, Peking University, Tianjin Binhai, China

18:25 Nov.6 **P3-6**

A 0.9V All Digital Synthesizable OPAMP with Boosted Gain and Widened Common Mode Input Range

Yiren Liu, Baijie Zhang*, Xu Cheng, Jun Han, Xiaoyang Zeng

State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

18:30 Nov.6 **P3-7**

Equivalent quantization correction technique for Pipelined SAR ADC

Ting Sun[1] , Qi Yu[1] , Yuyu Lin[1] , Chengze Li[1] , Jing Li[1] *, Ning Ning[1]

[1]State Key Lab of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China

18:35 Nov.6 **P3-8**

A Low Power, wide-band input buffer for 12bit 1GS/s ADC

Wenbin He, Ziwei Li, Fan Ye*, Junyan Ren

State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

18:40 Nov.6 **P3-9**

A Low Power Residue Amplifier using Incomplete Settled Differential Flipped Voltage Follower

Wenbin He, Ziwei Li, Min Chen, Fan Ye*, Junyan Ren

State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

18:45 Nov.6 **P3-10**

A 20MS/s 12b 737.76μW SAR ADC in 0.18μm CMOS

Yu-Ping Guo[1] , Jia-Qi Jiang[2] , Ning Ding[2] , Yu-Chun Chang[1] *

[1] State Key Laboratory on Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun, China; [2]School of Microelectronics, Dalian University of Technology, Dalian, China.

18:50 Nov.6 **P3-11**

An Inductor-Less Highly Linear LNA with Noise Cancelling and Current Reusing for 3-5 GHz Low-Power UWB Receivers

Wenli Shen[1] , Pengyu Liu[1,2], Sheng Zhang[1,2]*

[1]Shenzhen International Graduate School, Tsinghua University, Shenzhen, China; [2]Institute of Microelectronics, Tsinghua University, Beijing, China

18:55 Nov.6 **P3-12**

A 4Gbps DPPM On-chip Serial Link Based on Pipelined Vernier-TDC

Jinhao Li[1] , Chong Qu[2] , Fan Wu[2] , Jianfei Jiang[1]*

[1]Department of Microelectronics and Nanoscience, Shanghai Jiao Tong University, Shanghai, China; [2]China Shipbuilding Industry Corporation 711 Research Institute, Shanghai, China

19:00 Nov.6 **P3-13**

A 2.4GHz OOK Power Programmable CMOS RF Power Amplifier

Li-han Cui, He-Jia Cai, Tao Wang, Zhi-Liang Hong*

State Key Laboratory of ASIC & System, Fudan University, Shanghai, China

19:05 Nov.6 **P3-14**

A Dual-mode Digital Power Amplifier for 2.4GHz and 5GHz with 40.6dB Third-harmonic Suppression Ratio

Li-Han Cui*, He-Jia Cai, Tao Wang

State Key Laboratory of ASIC & System, Fudan University, Shanghai, China

19:10 Nov.6 **P3-15**

A Low-Power Compact Inductor-less RF Front-end for Sub-1GHz IoT Applications

Jing-Ye Zhang, Miao-Xing Xie * , Ren-Hua Liu, Ya-Bin Sun, Xiao-Jin Li, Shao-Hui Xu, Yan-Ling Shi

Shanghai Key Laboratory of Multidimensional Information Processing and the Department of Electrical Engineering, East China Normal University, Shanghai, China

19:15 **P3-16** Nov.6

A 28GHz 6-bit Two-stage Vector-sum Phase Shifter with Low RMS Error for 5G Mobile Communication

Xingyu Qi[1] , Shuyu Liu[1] , Zongyuan Zheng[1] , Bo Wang[1] *, Xing Zhang[2]

[1]The Key Lab of Integrated Microsystems, Peking University Shenzhen Graduate School, Shenzhen 518055, China; [2]School of Electronics Engineering and Computer Science, Peking University, Beijing, China

19:20 **P3-17** Nov.6

A Low-power VCO with Switch Current Source and Pseudo CML Frequency Divider for Bluetooth 5.0 Applications

Zirui Jin[1] , Dongsheng Liu[1]*, Ang Hu[1] , Mingyang Gong[2]

[1]School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, China; [2]Wuhan Runjet Electronic Technology Co., Ltd., Wuhan, China

19:25 **P3-18** Nov.6

A decimation filter for Sigma delta modulator in FMCW radar transceiver and the design methodology

Yue Lin[1]*, Jian Xu[1] , LinYing Dai[2]

[1]ICLegend Micro Co.,Ltd., Shanghai, China; [2]State Key Laboratory of ASIC and System, Fudan University, Shanghai, China

19:30 **P3-19** Nov.6

A Fast-Locking Near-Threshold All-Digital SARDLL

Tailong Xu, Sheng Zhang, Xueyou Hu*

Department of Electronic Information Engineering, College of Advanced Manufacture Engineering, Hefei

19:35 **P3-20** Nov.6

Design of A Wide-Range PLL Based on Dual VCO Technique for Sub-1G IoT Application

Ming Wang[1] , Miao-Xing Xie[1]*, Xiang-Long Li[1] , Ya-Bin Sun[1] , Xiao-Jin Li[1] , Yan-Fang Ding[1] , Yan-Ling Shi[1]

[1]Shanghai Key Laboratory of Multidimensional Information Processing and the Department of Electrical Engineering, East China Normal University, Shanghai, China

19:40 **P3-21** Nov.6

A 23-30.8GHz All-digital Phase-Locked Loop for 5G Communication System

Jieyang Li, Ting Yi*, Zhiliang Hong

State Key Lab. of ASIC and System, Dept. of Microelectronics, Fudan University Room 245, Microelectronic Building, NO. 825 Zhangheng Rd, Pudong District, Shanghai, China

19:45 **P3-22** Nov.6

A Mesh-based Self-adaptive NoC with Low-latency Reconfigurable Ring Clusters

Zhiheng Fan[1]*, Jianwei Yang[2] , Jun Han[3] *, Xiaoyang Zeng[4] , Xu Cheng[5]

Department of Microelectronics, Fudan University, Shanghai, China

19:50 **P3-23** Nov.6

Multi-parameter Timing Optimization for Pulsed-Latch Circuits

Xiao Di, Wai-Shing Luk*, Lingli Wang

State Key Laboratory of ASIC & System, Fudan University, Shanghai, China

19:55 **P3-24** Nov.6

Charge-plasma Based Negative Capacitance Junctionless Transistor With Sub-60mV/dec Subthreshold Swing and High Ion/Ioff Ratio

Long-Fei Li[1] , Hung-Chih Chin[2] , Lining Zhang[1] , Xinnan Lin[1]*

[1]The Shenzhen Key Lab of Advanced Electron Device and Integration, ECE, PKUSZ, Shenzhen, China; [2]Semiconductor Manufacturing International (Shenzhen) Corporation, Shenzhen, P.R.China

20:00 **P3-25** **Design and Comparison of FIR Filter Based on DSP Builder and HDL Coder**

Nov.6

Qin Huang, Zilin Wang*

School of Software and Microelectronics, Peking University, Beijing, China

20:05 **P3-26** **Net-distribution-based Routability Optimization In Global Placement**

Nov.6

Dingcheng Li[1] , Cong Li *[1] , Likang Tao[1] , Yiqi Zhuang[1] , and Gengjie Chen[2]

[1]School of Microelectronics, Xidian University, Xi'an, China; [2]Shenzhen Giga Design Automation Co., Ltd

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