# Voidless metal filling and elimination of metal diffusion in PVD barrier and seed process for high performance Cu interconnect

Zheng-Jun Hu[1,2], Xin-Ping Qu[1*], Hong Lin[2], Qing-Yun Zuo[2], Wei-Jun Wang[2], Ming Li[2], Shou-Mian Chen[2], Yu-Hang Zhao[2]

[1]State key lab of ASIC and system, School of microelectronics, Fudan University, Shanghai 200433, China,

[2]Shanghai IC R&D Center, Shanghai 201210, China

[*]Email: xpqu@fudan.edu.cn

**Abstract**

In this paper, barrier and seed process with physical vapor deposition (PVD) methods for Cu interconnect were developed for the 28 nm node generations. We show that metal filling can be improved by optimizing the seed process. Under non-optimized condition, metal diffusion can be observed, which is mainly caused by the resputter steps during PVD. By increasing the barrier thickness, the metal diffusion can be eliminated. In these demonstrations, we measure the electrical characteristics, including metal line resistance and line leakage (<10 pA).

## 1. Introduction

Barrier/liner deposition is one of the key process modules in Cu interconnect.[1] Extending current PVD tool capability is the cost-effect way for new generation development. However, in new technology generation development, non-optimized barrier and seed layer deposition would cause metal filling voids and other process defects.

In this paper, 28 nm node barrier and seed process were developed with current PVD tool used for 65/45nm node. The metal filling and metal diffusion issues were solved by tuning the barrier and seed process. Finally, we measured metal line resistances and line leakage current.

## 2. Experiment

Figure 1 gives the schematic flow of the metal 1 (M1) and metal 2 (M2) short loop integration and 12" wafers were used. The dielectric etching tool was from AMEC using an ADRIE chamber. The barrier/seed deposition tool was from Lam Inova, and the ECP tool was from Lam Sabre. After Cu ECP, the samples were subjected to CMP, using a tool from AMAT Reflexion LK. For the M1/M2 electrical quick test, nitrogen-doped silicon carbide (SiCN) capping layer was deposited after Cu CMP using a tool from Lam Vector.

The feature size of the metal line width in M1 and M2 was 45 nm and the pitch was 90 nm, Metal hard mask (MHM) integration was used. The film stack was SiCN/SiCOH/$SiO_2$/TiN, in which, SiCN, the bottom layer, was the Cu barrier and etching stop layer; SiCOH was low-k with k value of 2.55; the $SiO_2$ layer was the insulator between the low-k dielectric and TiN was the metal hard mask. In the MHM approach, the trench was defined by patterning and etching TiN. The M1 structure was formed after TiN opening and etching the dielectric. In M2 development, after TiN opening and via lithography, the via and trench structure in the low-k dielectric were formed by the dielectric etching process.

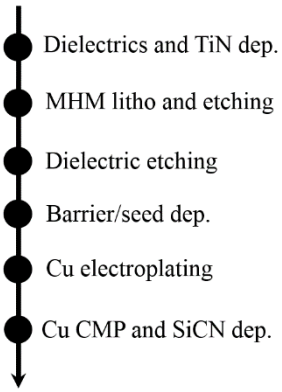


Figure 1. Schematic flow of M1 and M2 short loop

Metal filling and diffusion were checked by transmission electron microscopy (TEM) and scanning electron microscopy (SEM), and the elemental composition of the metal filling was checked by electron energy-loss spectroscopy (EELS). The TEM samples were prepared with a focused ion beam (FIB). After dielectric etching and metal filling, metal line resistance and leakage current with line width 45nm and pitch 90nm of M1 and M2 were measured respectively.

## 3. Results and discussions

### 3.1 Metal Filling

By using PVD deposition condition of the 65/45nm node, it was found that voids appeared after the Cu ECP process in M1 feature structure (metal line width 45nm, pitch 90nm). To clarify whether the voids came from PVD or ECP, we performed PVD deposition alone. From Figure 2 (a), it was shown clearly that the structure was already sealed after PVD deposition, and Cu

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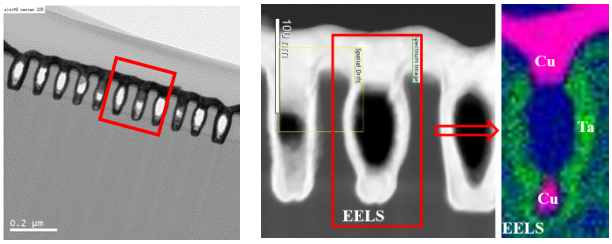
accumulated and sealed the top of the structure from EELS results in Figure 2 (b).




(a) (b)

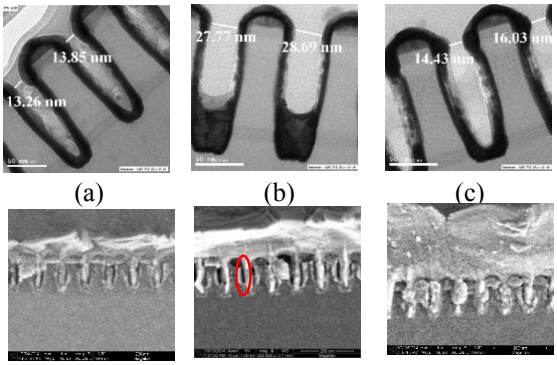
Figure 2. (a) TEM image after barrier/seed PVD deposition using 65/45nm node condition (b) EELS results of TEM image

Three kinds of barrier/seed processing conditions were designed, which aimed to improve the opening of the structure top by thinning the Cu seed. The detail conditions with 65/45nm node condition are shown in Table 1. Same final barrier thickness is adopted in all three conditions while for PVD-A condition the thickness of barrier and resputter is greater than those for PVD-B and PVD-C condition. Same Cu seed process condition is used in the PVD-A and PVD-C conditions. It was reported that Cu reflow was in favor of metal filling and Cu reflow was tried in the PVD-B condition [2] After Cu seed deposition, the wafer was transferred to the preclean chamber at 250°C without breaking vacuum, and then was annealed for 1 min.

Table 1. The summary of opening and various PVD process conditions of M1

| Barrier/seed steps | 65/45nm Node | PVD-A | PVD-B | PVD-C |
|---|---|---|---|---|
| Barrier-dep. (Å) | 220 | 100 | 60 | 60 |
| Barrier-resp.(Å) | 50 | 60 | 20 | 20 |
| Final barrier Thi. (Å) | 170 | 40 | 40 | 40 |
| Seed-Dep. (Å) | 500 | 130 | 170 | 130 |
| Seed-respu. (Å) | 0 | 50 | 50 | 50 |
| Seed-final (Å) | 500 | 80 | 120 | 80 |
| Opening (nm) | 0 | 13.56 | 28.23 | 15.23 |

Figure 3 shows the TEM and SEM images of using various PVD conditions in Table 1. From the SEM images in Figures 3 (d), (e) and (f), voidless Cu filling were achieved after ECP process. The opening of structure was measured from Figures. 3 (a), (b) and (c) and summarized in Table 1. The opening of feature structure is 13.56 nm, 28.23 nm, 15.23 nm for PVD-A, PVD-B, and PVD-C respectively. Less opening was achieved after PVD-A condition. This was probably due to the more barrier deposition caused less opening in spite of the same final barrier thickness. The seam (red circle in Figure 3 (e)) was observed in the sidewall of trench between metal and dielectrics after ECP deposition with PVD-B conditions. This phenomenon supposed that less Cu continuity occurred before Cu ECP. It could be explained that: before reflow, the thinnest Cu thickness was in the middle of the structure; after reflow, less Cu exist in the top and middle of the structure which resulted in the less Cu continuity. Finally, PVD-C condition is chosen for its voidless filling and larger opening.




(a) (b) (c)

(d) (e ) (f)

Figure 3. TEM images for samples after PVD deposition using (a) PVD-A; (b) PVD-B; and (c) PVD-C; and SEM images after ECP process using (d) PVD-A ; (e) PVD-B; and (f) PVD-C

### 3.2 Metal Diffusion

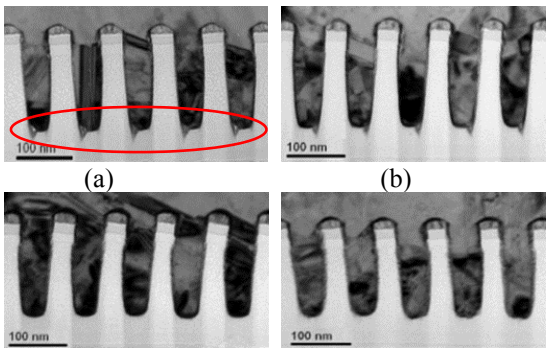
Metal diffusion is observed in the bottom of M2 feature structure (metal line width 45nm, pitch 90nm) from the TEM results (red circle in Figure 4 (a)) after PVD and ECP process. Metal diffusion has been reported as microtrenching caused by the TaN/Ta etch, which was suggested as a result of Cu and Ta particles penetration into the dielectrics. [3] The barrier thickness was varied to check whether the metal diffusion phenomenon could be improved. In Table 2, three PVD conditions experiments (EXP-1, EXP-2, EXP-3) were designed with different the Ta and TaN thickness and the baseline (BL) condition was given. The same Cu seed and resputter conditions were performed for these four conditions. After PVD barrier and seed processes in Table 2, the same Cu electroplating processes were performed.

The barrier deposition for the Cu interconnect has four steps: TaN deposition, 1st Ta deposition, resputter by Ar ions, and 2nd Ta deposition. During resputter, the bottom of the feature structure was bombarded by the Ar ions, causing the bombarded barrier material to redeposit on the sidewall of the bottom structure, which not only

improved the sidewall coverage near the bottom but also decreased the via contact resistance. Figure 4 shows the TEM image of various PVD conditions after ECP process. In comparing Figures. 4 (a) and (b), it shows that increasing the TaN thickness could alleviate the metal diffusion and with increased 2nd Ta deposition thickness (Figure 4 (d)), no metal diffusion appeared. Also, metal diffusion did not appear without using resputter, as shown in Figure 4 (c). The lack of metal diffusion in Figure 4 (c) may imply that the resputter process caused metal diffusion into the low-k dielectric. During resputter, Ar ions are vertically accelerated to bombard the barrier material at the bottom. Also, the corner effect from charge accumulation may cause local damage at the bottom corner of the feature structure. The corner damage is exacerbated by the weak physical hardness of the porous low-k dielectric. In the following copper ECP, copper could punch through the weaker interface between barrier and porous SiCOH at the corner. After increasing the thicknesses of the TaN and 2nd Ta deposition, metal diffusion could be eliminated, even with the barrier and Cu resputter.

Table 2. metal diffusion experiment of various PVD conditions in M2 (unit: Å)

| Barrier/seed steps | BL | EXP-1 | EXP-2 | EXP-3 |
|---|---|---|---|---|
| TaN dep. | 20 | 30 | 30 | 30 |
| 1st Ta dep. | 20 | 20 | 50 | 20 |
| Respu. | 20 | 20 | N.A. | 20 |
| 2nd Ta dep. | 20 | 20 | N.A. | 30 |
| Cu dep. | 170 | 170 | 170 | 170 |
| Cu respu. | 50 | 50 | 50 | 50 |
| Cu final | 120 | 120 | 120 | 120 |



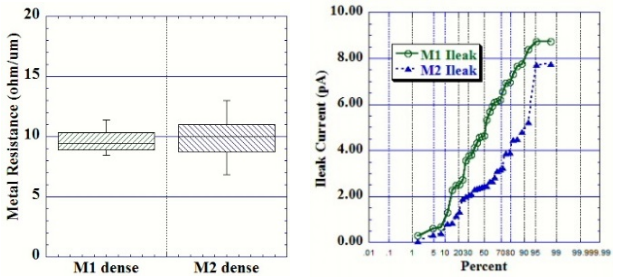

(a) (b)

( c ) ( d )

Figure 4. TEM image after ECP process with PVD deposition (a) BL (b) EXP-1 (c) EXP-2 (d) EXP-3

### 3.3 Metal Resistance and Line leakage of M1 and M2

After metallization of M1 with PVD-C condition (Table 1) and M2 with EXP-3 conditions (Table 2), we measured the electrical characteristics, including metal dense line per μm and line leakage current on the feature structure of metal line with width of 45 nm and pitch 90 nm. As shown in Figure 5 (a), the average metal resistances per μm of M1 and M2 were 9.65 and 9.91 Ω/μm respectively, which were comparable with the result 9.5ohm/μm in the literature. [4] The leakage current of M1 and M2 were all below 10 pA, as shown in Figure 5 (b).




(a) (b)

Figure 5. (a) Metal resistance per μm of M1 and M2 with feature structure metal line width 45nm and pitch 90nm (b) Metal line leakage of M1 and M2 with feature structure metal line width 45nm and pitch 90nm

### 4. Conclusion

Barrier/liner process was successfully developed for the metal line width 45nn and pitch 90nm in 28nm node. Full metal filling was achieved by decreasing the seed thickness. With proper barrier thickness adjusting, metal diffusion was eliminated. Electrical results on M1 and M2 metal line resistance, and line leakgae current are demonstrated.

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